



SPLC 2009

Università degli Studi di Udine
Dipartimento di Ingegneria Elettrica,
Gestionale e Meccanica



Third Workshop on Power Line Communications

October 1 – 2, 2009 – Udine – Italy



WSPLC 2009 Programme

Technical Sponsors



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Initiative co-founded by Agemont within the project "Fillera ICT (Regione Friuli-Venezia-Giulia) L.R. 2/2006 art.8"



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WSPLC 2009

Programme and Practical Information

Welcome to the Third Workshop on Power Line Communications
in Udine!

Workshop website: <http://www.diegm.uniud.it/wsplc09/>

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Workshop supported by

- *IEEE PLC Technical Committee*
- *IEEE ISPLC Steering Committee*
- *IEEE Italy Section*
- *Italian National Telecommunications and Information Theory Group (GTI)*
- *Agenzia per lo Sviluppo Economico della Montagna (Agemont)*
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- *Friuli Innovazione*
- *Università degli Studi di Udine*
- *Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica (DIEGM)*
- *Associazione Laureati in Ingegneria Elettronica (ALIE)*

Message from the WSPLC Chair

It is my great pleasure to welcome you to the Third Workshop on Power Line Communications. This year WSPLC is hosted by the University of Udine, Italy, after the previous two events held at the University of Dresden, Germany, and at the University of Thessaloniki, Greece.

Udine is the capital of the homonymous province in the beautiful region of Friuli-Venezia-Giulia, a region located in Northeastern Italy, between the borderlines of Austria and Slovenia where you can enjoy the Alps and the Adriatic sea. The University of Udine is one of the top ranked universities in Italy. It has been founded in 1978 and it enrolls about 17.000 students.

The workshop central theme is Signal Processing and Channel System Modeling in PLC, two important research areas for the development of PLC systems and for granting the successful evolution and improvement of existing technology. The technical program committee has coordinated the review process for the selection of the papers to be presented and published in the proceedings. The program includes six oral sessions and one parallel poster session whose topics are channel modeling, signal processing, modulation, resource allocation, and system applications and implementations. A keynote speech discussing DSL technology is offered to promote cross-fertilization among related fields and technologies. Furthermore, a tutorial on PLC covering advances in the development of Gbps in-home PLC networks has been organized by participants to the EU FP7 Project OMEGA.

I sincerely wish to thank the TPC committee members, F. J. Cañete, J-P. Javaudin, S. Galli, L. Lampe and P. Siohan, for their work in the review process, and also S. D'Alessandro and M. Biondi for their great help in the local arrangements.

I also wish to thank the technical support of IEEE Italy Section, of the Italian National Telecommunications and Information Theory Group GTTI, the IEEE Technical Committee on PLC (TC-PLC), and the IEEE ISPLC Steering Committee.

A deep thank goes to the sponsors AGEMONT, Fondazione CRUP, and Friuli Innovazione whose generous contribution helped significantly reduce the registration fees.

Andrea M. Tonello
WSPLC 2009 Chair

Committee

Chair

Andrea M. Tonello (University of Udine, Italy)

Technical Program Committee

Francisco J. Cañete (University of Málaga, Spain)

Stefano Galli (Panasonic, USA)

Jean-Philippe Javaudin (France Telecom - Orange Labs, France)

Lutz Lampe (University of British Columbia, Canada)

Pierre Siohan (France Telecom - Orange Labs, France)

Local Arrangements

Milena Biondi (University of Udine, Italy)

Salvatore D'Alessandro (University of Udine, Italy)

Venue Map



Workshop Site

Palazzo Antonini, Piazza Antonini 8, "Aula 7"

Social Event Site

Casa della Contadinanza, Udine Castle

Lunch

Caffè Caucigh, Via Gemona 36, Udine

Practical Information

How to reach the workshop site

By foot

The workshop site is at walking distance from most of the hotels located in the city centre. See the map on WSPLC 2009 web site at <http://www.diegm.uniud.it/wsplc09/Venue.html>

Bus

Line 1 with stop in San Cristoforo square. For information and timetable see <http://www.saf.ud.it/ricercaorari2.aspx?area=UD>

Taxi

RADIOTAXI, phone: (+39) 0432 503400

Venue details

Oral sessions

Room: Aula 7, Palazzo Antonini, Piazza Antonini 8, Udine

Poster sessions

Room: Sala Atti, Palazzo Antonini, P.zza Antonini 8, Udine

Lunch

Caffè Caucigh, Via Gemona 36, Udine

Social event

Casa della Contadinanza, Udine castle.

Internet access

WLAN connection is available. Ask for support at the registration desk.

Program Time-table

Thursday, October 1st, 2009

- 8.00-8.40 Registration
- 8.40-9.00 **Welcome Message and Introduction**
prof. A. F. De Toni, Dean of the Faculty of Engineering,
prof. A. M. Tonello, WSPLC 09 Chair, University of Udine, Italy
- 9.00-10.20 Session A: **Channel Modeling I**
chair: F. J. Cañete, University of Málaga, Spain
- 10.20-10.50 Coffee Break and Session B (Poster): **System Implementations and Applications**
chair: M. Katayama, Nagoya University, Japan
- 10.50-11.50 Keynote Speech: **Future and Challenges of DSL Systems, Dr. Axel Clausen**, Infineon Technologies, Austria
- 11.50-12.30 Session C: **Multicarrier Modulation Part I**
chair: S. Weiss, University of Strathclyde, Scotland
- 12.30-14.00 **Lunch**
- 14.00-15.00 Session D: **Multicarrier Modulation Part II**
chair: P. Siohan, France Telecom - Orange Labs, France
- 15.00-15.20 Coffee Break and Session B (Poster): **System Implementations and Applications**
- 15.20-18.00 PLC Tutorial: **Advances towards Gbps In-Home PLC Networks: The OMEGA Project**
Chair: A. M. Tonello, University of Udine, Italy
- 19.30-22.30 **Social Event**

Friday, October 2nd, 2009

- 8.00-8.40 Registration
- 8.40-9.00 Warm-up and Free Technical Discussion
- 9.00-10.20 Session E: **Channel Modeling II**
chair: P. Pagani, France Telecom - Orange Labs, France
- 10.20-10.50 Coffee Break and Session B (Poster): **System Implementations and Applications**
chair: A. M. Tonello, University of Udine, Italy
- 10.50-12.30 Session F: **Signal Processing and Analysis**
chair: J. A. Cortés, University of Málaga, Spain
- 12.30-14.00 **Lunch**
- 14.00-15.20 Session G: **Systems, Applications and Resource Allocation**
chair: R. Lehnert, University of Dresden, Germany
- 15.20-15.45 Coffee Break and Session B (Poster): **System Implementations and Applications**
- 15.45-16.00 Workshop Closure
- 16.30-18.30 **Guided Tour**

Technical Sessions

Session A: Channel Modeling I

(Thu. 1 Oct., 9.00-10.20)

1. **MIMO Capacity of Inhome PLC Links up to 100 MHz**
R. Hashmat (1), P. Pagani (1), T. Chonavel (2), (1: Orange Labs, France), (2: Telecom Bretagne, France)
2. **Simulation of Channel Characteristics for Complex Networks**
A. Lehmann, K. Kolle, (Ahrus University, Denmark)
3. **New Results on Top-Down and Bottom-Up Statistical PLC Channel Modeling**
A. M. Tonello, F. Versolatto, (University of Udine, Italy)
4. **Characterization of PLC Communication Channel: A Networking Perspective**
E. Malacasa, G. Morabito, (University of Catania, Italy)

Session B (Poster): System Implementations and Applications

(Thu. 1 Oct., 10.20-10.50 and 15.00-15.20

Fri. 2 Oct., 10.20-10.50 and 15.40-16.00)

1. Communication Architecture of Smart Grids to Manage the Electrical Demand

R. Mora (1), A. Lopez. (2), D. Roman (2), A. Sendin (3), I. Berganza (3), (1: SIEMENS, Spain), (2: CEDETEL, Spain), (3: IBERDROLA, Spain)

2. A Novel Multi-power Silicon Platform for PRIME Full System Integration in a SingleChip

A. Lasciandare (1), S. Bois (1), P. Bisaglia (1), A. Moscatelli (2), (1: DORA, Italy), (2: STMicroelectronics, Italy)

3. Design and Test of a Microcontroller Peripheral for Grid-Aware Networked Digital Appliances

A. Ricci (1), B. Vinerba (2), E. Smargiassi (2), I. De Munari (1), V. Aisa (2), P. Ciampolini (1), (1:University of Parma, Italy), (2: Indesit Company, Italy)

4. Gateways between Broadband and Narrowband Power Line Communication Systems – Solutions for Multimedia Devices

P. Lucchini, M. Lutman, M. Capobianco, (SIPRO, Italy)

5. New Proposed Integrated System of Visible Free Space Optical with PLC

S. E. Alavi, A. S. M. Supa 'at, S. M. Idrus, S. K. Yusof, (Universiti Teknologi Malaysia, Malaysia)

6. A Very Low Area ADC Architecture Capable of Supporting the Analog Front End of Powerline Communication Systems

N. Petrellis, M. Birbas, J. Kikidis, A. Birbas, (Analogies S.A., Greece)

7. Power Line Channel Models: Comparisons Between Different Modeling Adopted in BPLC Systems

J. Anatory (1), N. Theethayi (2), N. H. Mvungi (1), (1:University of Dodoma, Tanzania), (2: Uppsala University, Sweden)

8. Efficient and Reliable Power Line Communications Through Coding and Diversity Techniques

Z. Shi (1), J. Li (2), (1: University of Chengdu, China), (2: University of Bethlehem, PA, U.S.A)

Session C: Multicarrier Modulation Part I

(Thu. 1 Oct., 11.50-12.30)

1. Some (Known) Facts on Multicarrier Communication

R. Raheli (1), M. Franceschini (2), R. Pighi (3), G. Ferrari (1), (1: University of Parma, Italy), (2: IBM T. J. Watson Research Center, USA), (3: Selta, Italy)

2. HS-OQAM PLC: Long Prototype Filter or Equalizer?

H. Lin, P. Siohan, (France Telecom, France)

Session D: Multicarrier Modulation Part II

(Thu. 1 Oct., 14.00-15.00)

3. An Oversampled Modulated Filter Bank Transmultiplexer with Precoding and Equalisation

S. Weiss, P. Yarr, W. Al-Hanafy, A. P. Millar, C-H Ta, (University of Strathclyde, Scotland)

4. Coded OFDM vs. Wavelet-OFDM and Circular Wavelet-OFDM for Power Line Communications

L. Zbydniewski, T. P. Zielinski (AGH University of Science and Technology, Poland)

5. Performance Analysis of Asynchronous MC-CDMA Long Sequences for PLC Systems with Impulsive Noise

I. Val (1), F.J. Casajús-Quirós (2), (1: Ikerlan-IK4, Spain), (2: ETSIT Public University of Madrid, Spain)

Session E: Channel Modeling II

(Fri. 2 Oct., 9.00-10.20)

- 1. High-frequency Characterization of a Medium Voltage PLC Transmission System**
F. Campagna, M. Quarantelli, R. Pighi, (Selta, Italy)
- 2. Effect of MV/LV Transformer Substations on MV Power Line Signals Propagation**
C. Tornelli, L. Capetta, (ERSE, Italy)
- 3. PLC Technology: Characteristics of the Radiated Field and TEMPEST Considerations**
L. Diquelou, P. Laly, L. Kone, P. Degauque, (University of Lille, France)
- 4. PLC in Aircraft: Channel Modeling**
I. Junqua (1), V. Degardin (2), M. Lienard (2), S. Bertuol (1), P. Degauque (2), (1: ONERA DEMR, France), (2: University of Lille, France)

Session F: Signal Processing and Analysis

(Fri. 2 Oct., 10.50-12.30)

- 1. Distortion Evaluation of DMT Signals on Indoor Broadband Power-line Channels**
J. A. Cortés, L. Díez, F. J. Cañete, J. T. Entrambasaguas, (University of Málaga, Spain)
- 2. Phase Compensation for Narrowband PLC Channels with Cyclic Time-Varying Features**
Y. Sogiura, T. Yamazato, M. Katayama, (Nagoya University, Japan)
- 3. Using the Outdoor Lighting Infrastructure for Wireless Services**
M. Chiani (1), E. Paolini (1), A. Giorgetti (1), A. Grossi (2), M. Pensalfini (2), (1: University of Bologna, Italy), (2: UMPI R&D, Italy)
- 4. Modulation Diversity in Wideband In-Home PLC**
H. Lin, P. Siohan, (France Telecom, France)

Session G: Systems, Applications and Resource Allocation

(Fri. 2 Oct., 14.00-15.20)

- 1. Power-constrained Physical-Layer Goodput Maximization for PLC Links**
M. Biagi, E. Baccarelli, N. Cordeschi, V. Polli, T. Patriarca, (University of Rome, Italy)
- 2. Bit Rate Maximization for Multicast LP-OFDM Systems in PLC Context**
A. Maiga, J-Y. Baudais, J-F. Helard, (IETR/INSA, France)
- 3. Channel Reuse Improvement for Coexistence between Access and In-Home PLC Systems with Dynamic Resource Allocation**
L. P. Do, R. Lehnert, (University of Dresden, Germany)
- 4. Future High Speed In-Vehicle PLC Networks**
F. Nouvel, P. Tanguy, (IETR/INSA, France)

