

Channel Debiasing and Gate Current modelling in Advanced CMOS Devices

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Compact Modelling Solution for Advanced Devices

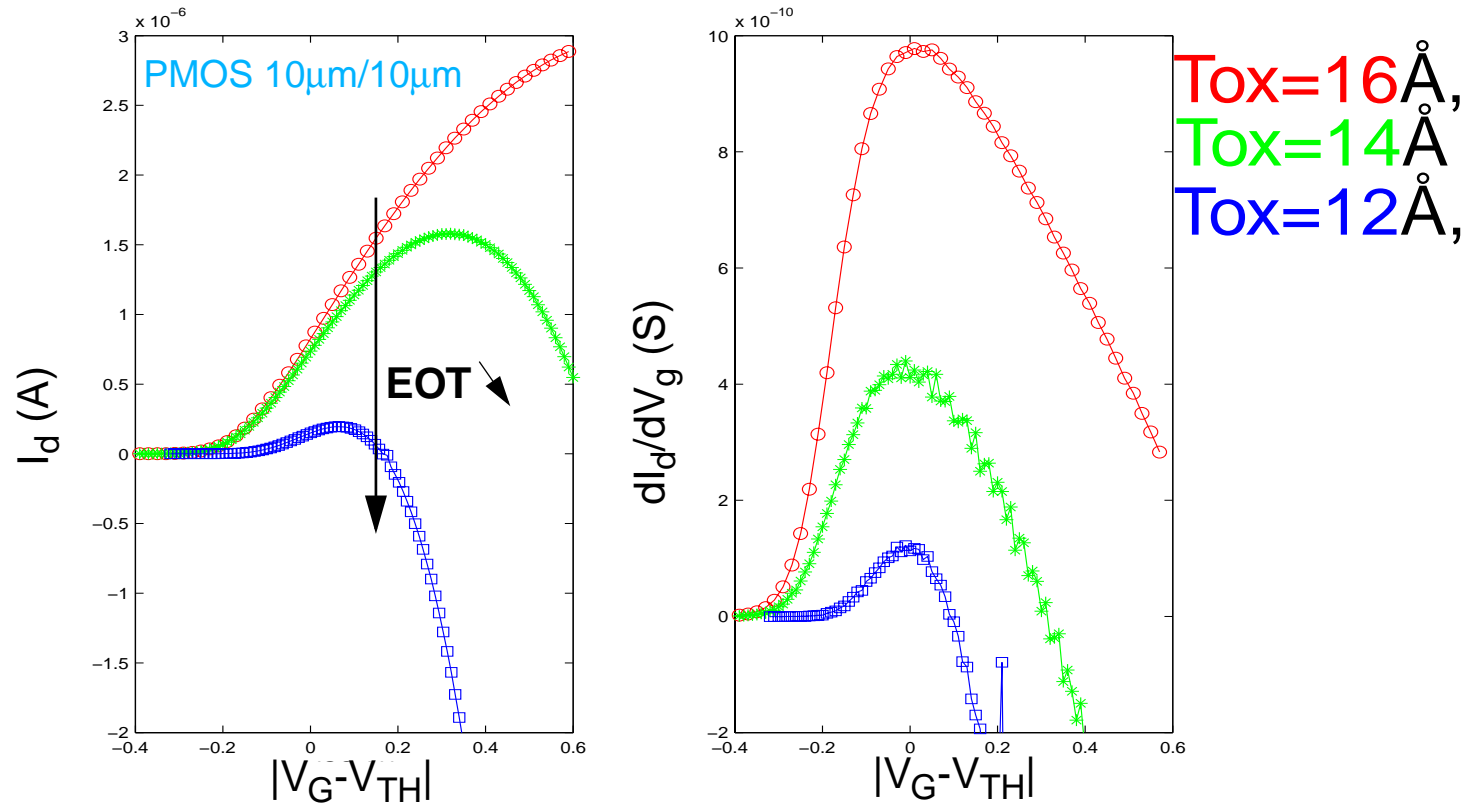
- ❑ Gate leakage exceeds $10\text{A}/\text{cm}^2$ in advanced MOS transistors ($T_{\text{ox}} < 14\text{\AA}$).
- ❑ The impact of this leakage on MOS DC and AC characteristics is still an open issue.
- ❑ Gate current correction for I(V) curves for device modelling and process monitoring purposes.
- ❑ Gate current compact modelling solution.

Outline

- ❑ Experimental Overview
- ❑ Model Derivation
- ❑ Discussion
- ❑ Application

Experimental:
Typical DC Characteristics of MOSFETs with gate leakage

$I_D(V_G)$ curves: Experimental (1/2)

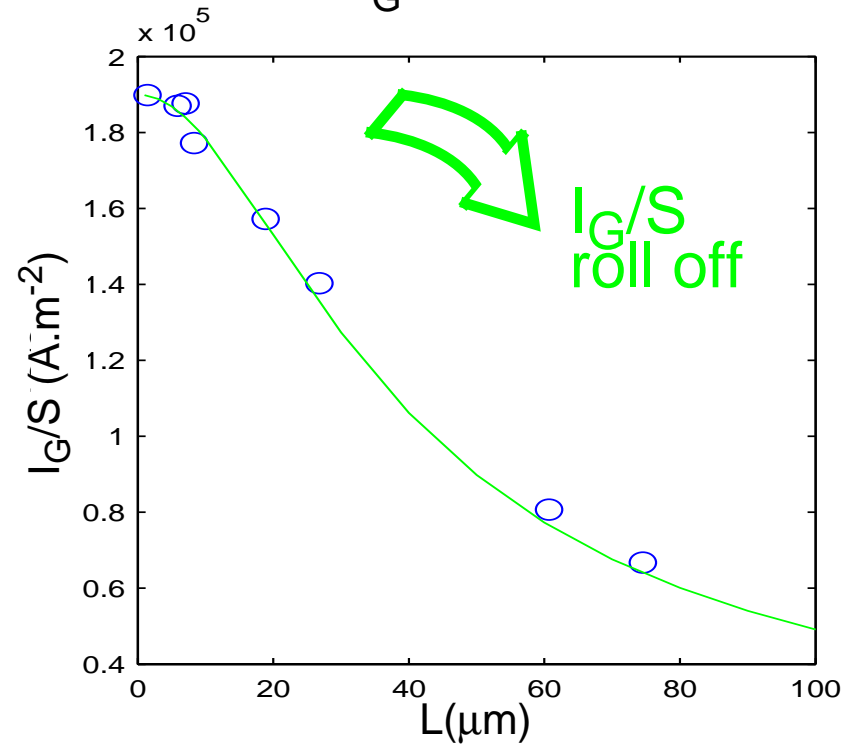
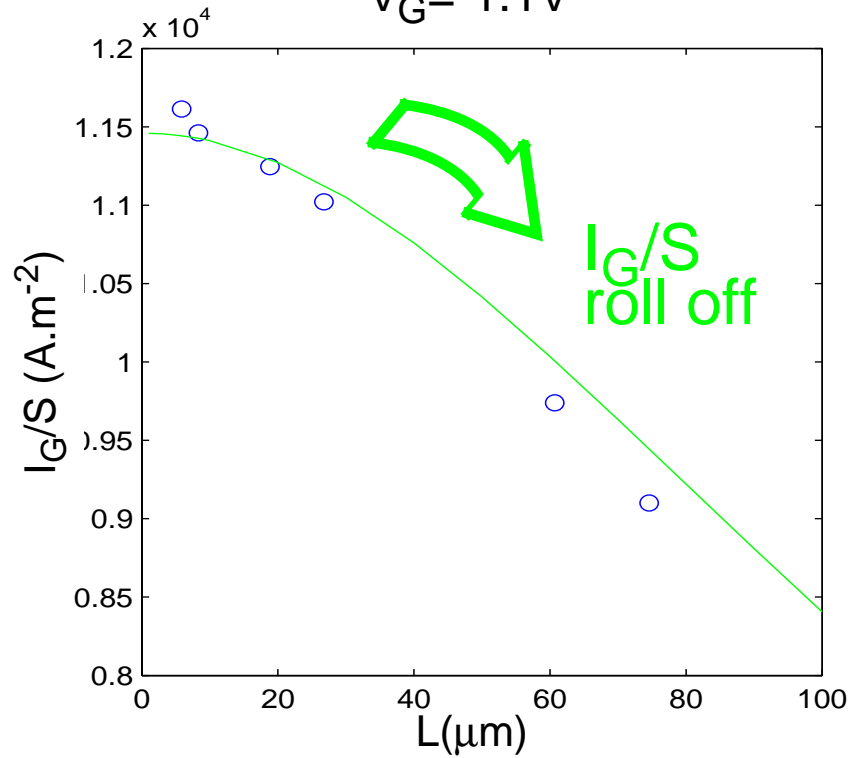


$I_D(V_G)$ & Transconductance; $V_B=V_S=0$ $V_D=-50\text{mV}$; HP4156; 27°C

Area Gate Current density: Experimental (2/2)

$T_{Oxeff}=15\text{\AA}$
 $V_G=-1.1V$

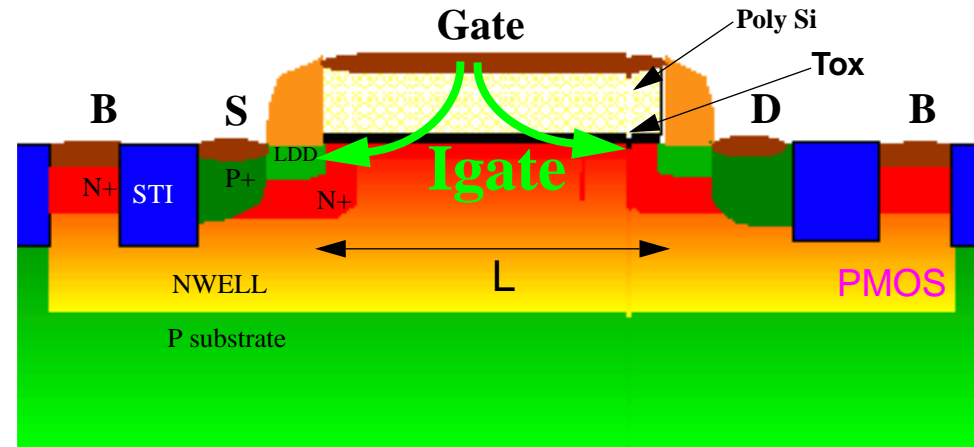
$T_{Oxeff}=13\text{\AA}$
 $V_G=-1.1V$



PMOS; $V_B=V_S=V_D=0$; HP4156; 27°C

Problem to Solve & Models

Problem to Solve (1/5)



➡ **How to describe the impact of gate leakage on transistor DC characteristics?**

Channel length dependent DC area gate current

➡ **What is the gate-to-drain and gate-to-source current partition?**

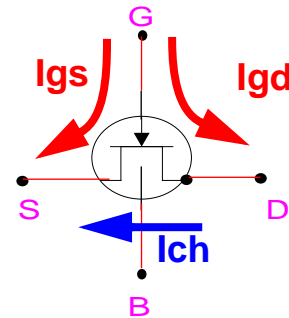
Accurate correction for first order parameters extraction

Models (3/5): Compact MOS model + gate leakage

Compact MOS model:

- $I_{channel}$ does not depend on gate leakage
- Gate leakage as:
- Charge sheet model

$$\begin{cases} I_{ch} - I_{GD} = I_D \\ I_{ch} + I_{GS} = I_S \end{cases}$$



☞ J.R. Brews, Solid state Electronics, 1978. Vol21 pp345-355

Models (4/5): Compact MOS model + gate leakage + series resistance

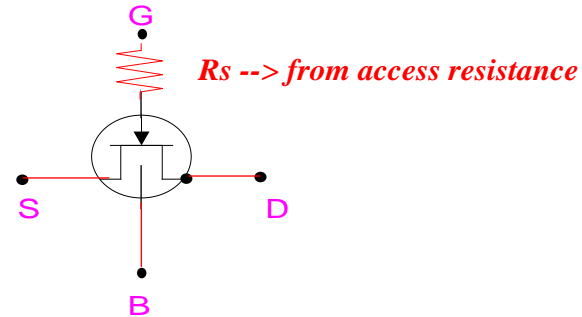
a) Model tentative

- $I_{channel}$ does not depend on gate leakage

- Gate leakage as:

$$\begin{cases} I_{ch} - I_{GD} = I_D \\ I_{ch} + I_{GS} = I_S \end{cases}$$

- Series access resistance to attempt to reproduce I_G/S roll off.



Models (5/5): Segmented model

b) Our work: segmented surface potential model.

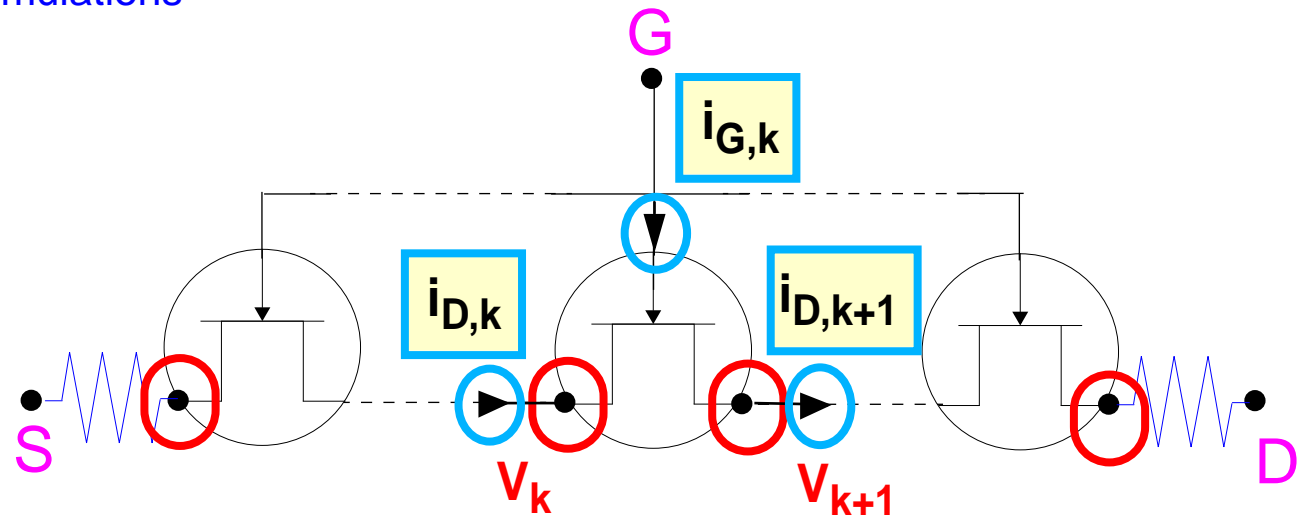
- Distributed gate leakage along the channel
- Channel divided into segments:

Unknowns: V_k

Continuity equation:

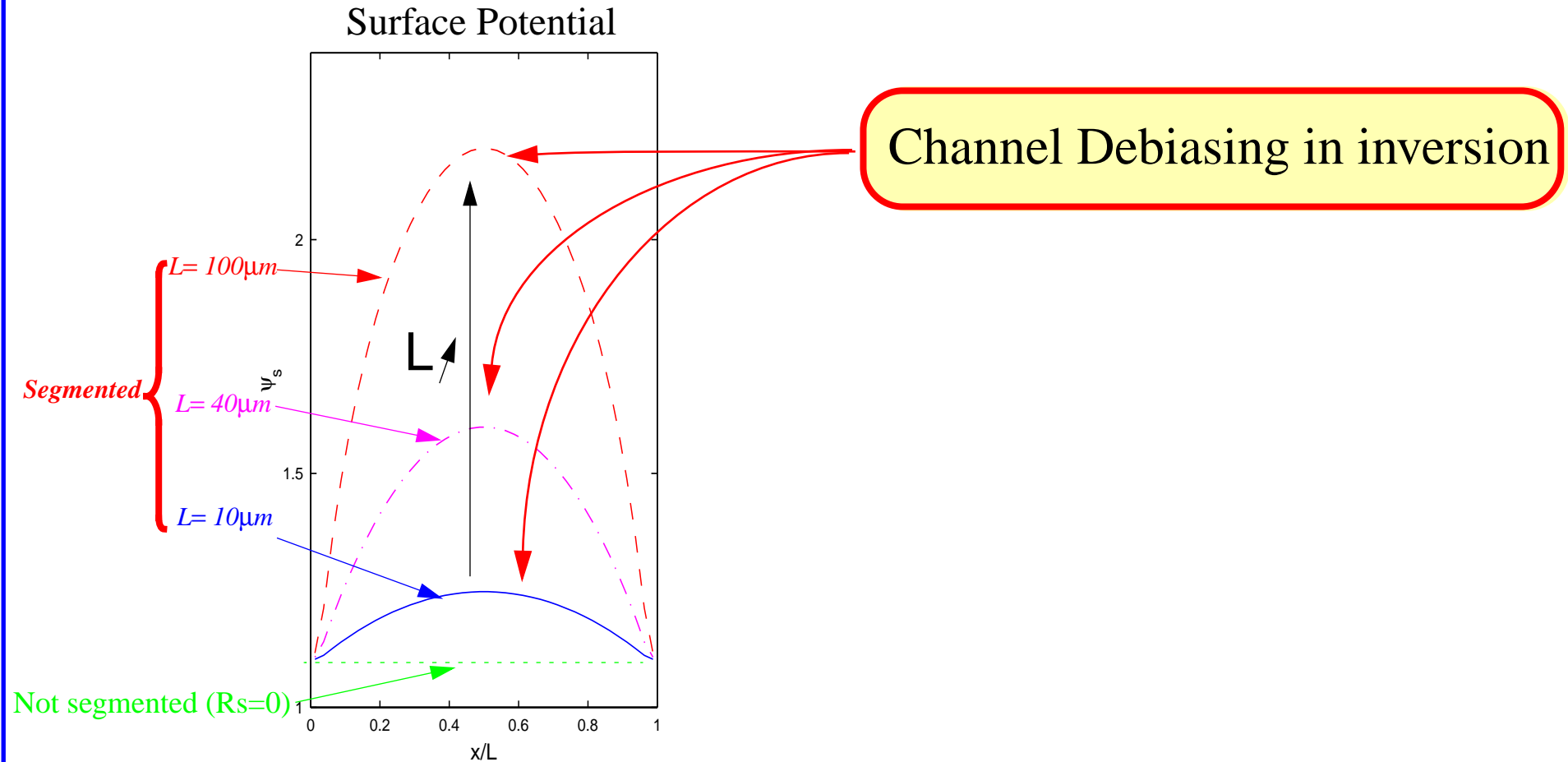
$$i_{D,k+1} - i_{D,k} = i_{G,k}$$

- For DC and AC simulations



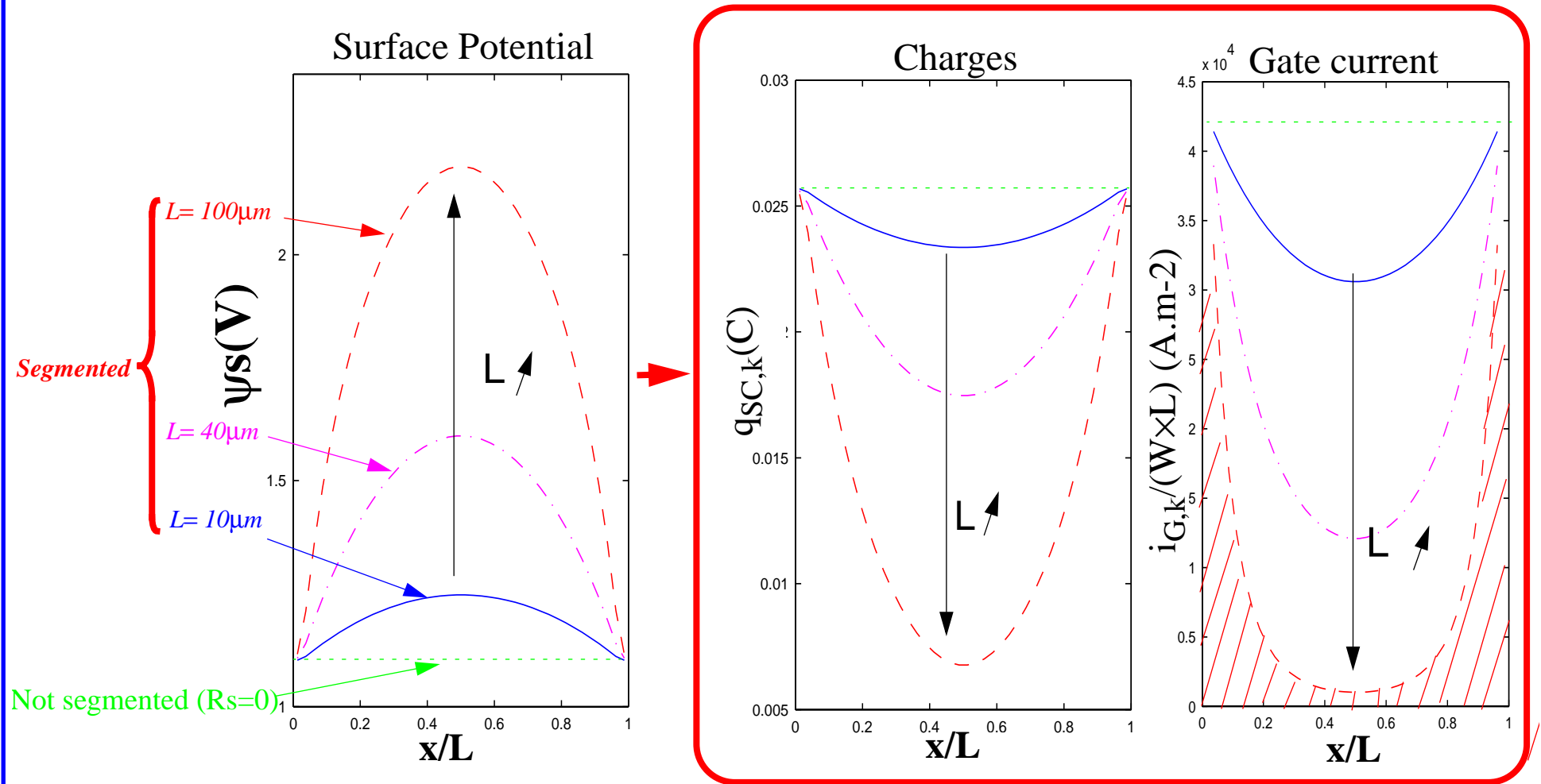
Discussion & Model Comparison

Model Comparison (1/4): Channel Debiasing on long Devices



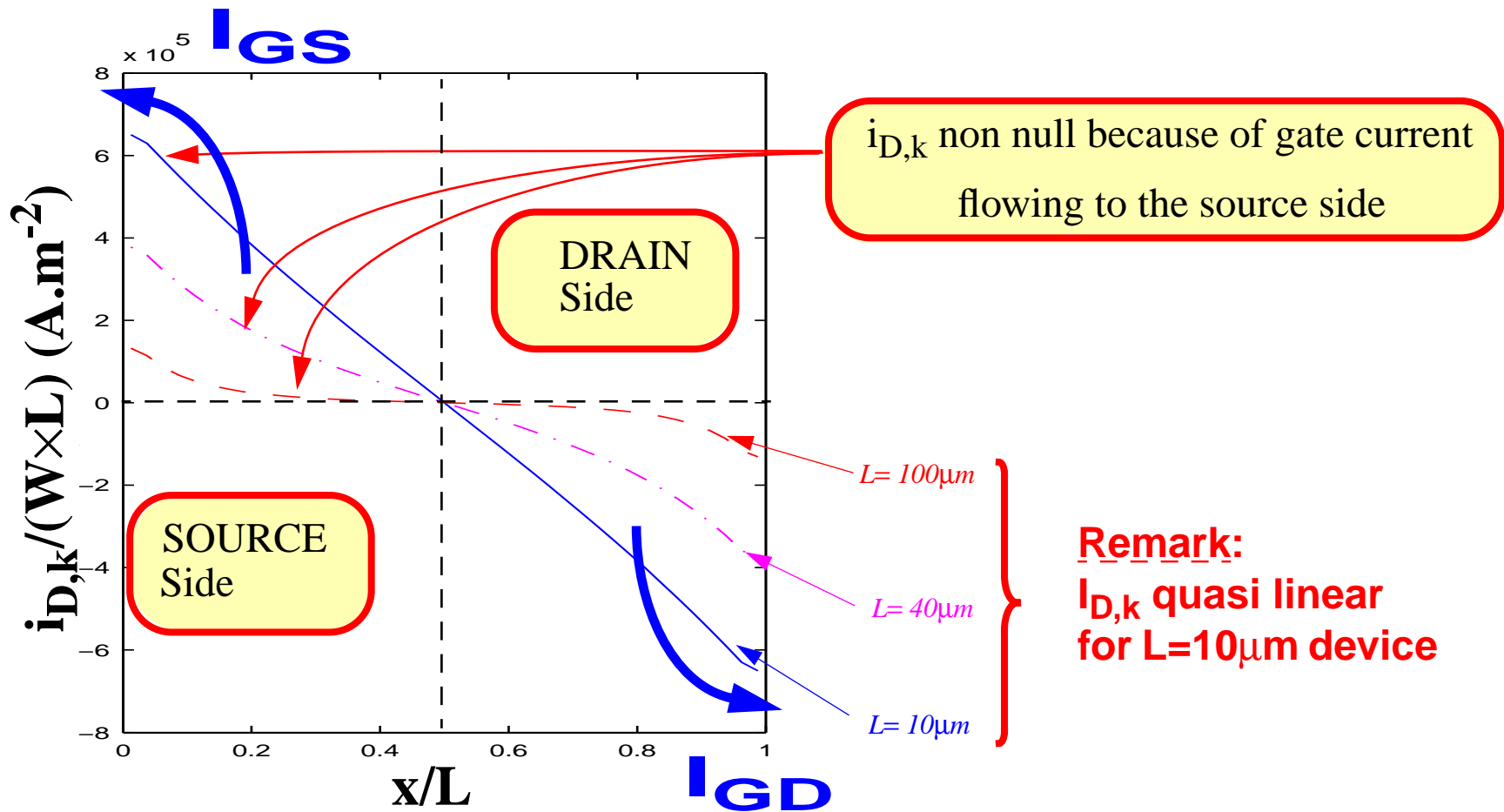
Simulation: $V_G=1.1V$; $V_B=V_S=V_D=0$; $27^\circ C$ $T_{ox,eff} = 13\text{\AA}$

Model Comparison (2/4): Channel Debiasing on long Devices



Simulation: $V_G=1.1V$; $V_B=V_S=V_D=0$; $27^\circ C$ $T_{ox,eff} = 13\text{\AA}$

Model Comparison (3/4): Channel Debiasing on long Devices (DC Analysis)



Simulation: $V_G = -1.1V$; $V_B = V_S = V_D = 0$; $27^\circ C$ $T_{ox\,eff} = 13\text{\AA}$

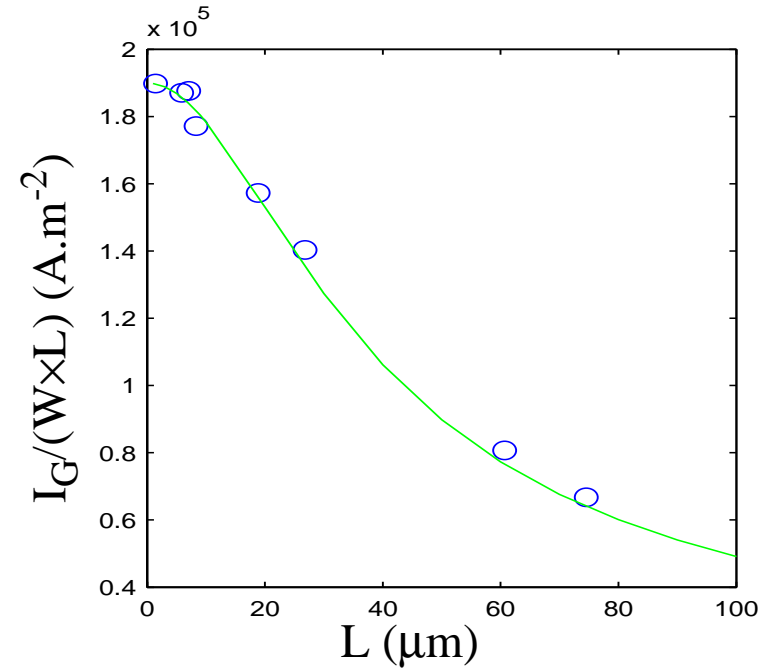
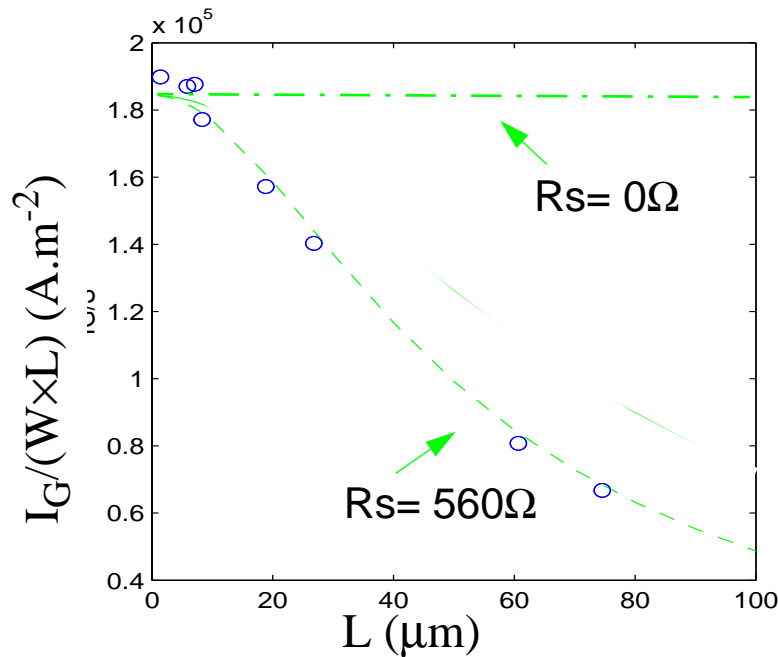
Model Comparison (4/4): Area gate current (DC Analysis)

a) Charge Sheet model + series resistance

b) Segmented Charge Sheet model

$V_G = -1.1V$

$V_G = -1.1V$



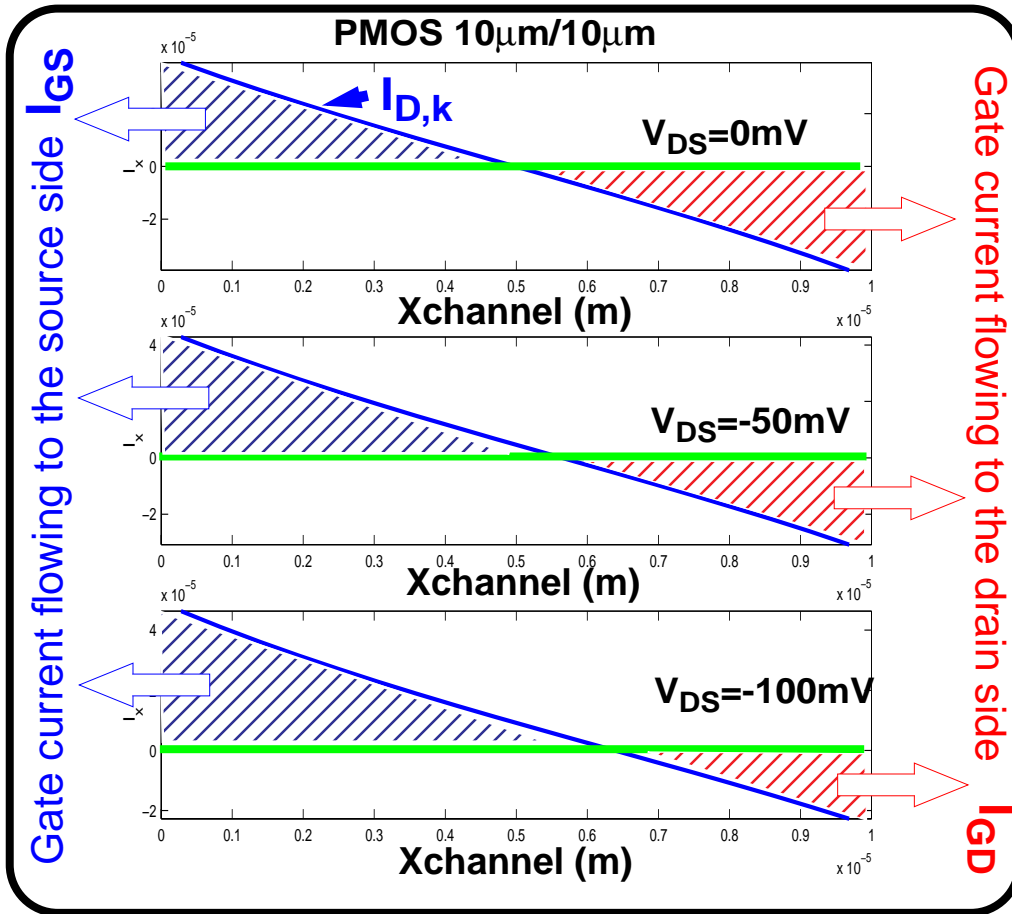
**No unique value for all Vg
Values have no physical meaning**

**Fits for all Vg
Only geometry parameters**

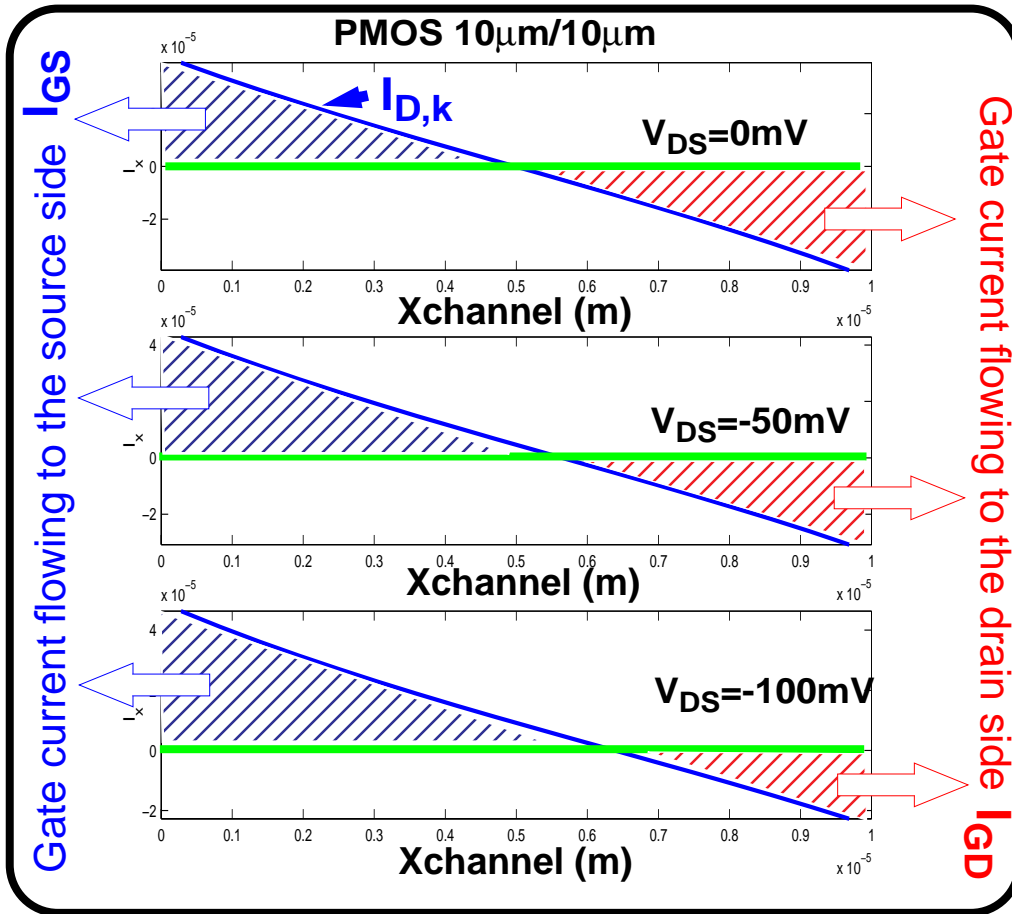
HP4156 Measurements & simulations; $V_B = V_S = V_D = 0$; 27°C; $T_{ox,eff} = 13\text{\AA}$

Model application: Gate current partitioning

Model Application (1/4): Gate current partitioning calculation methods



Model Application (1/4): Gate current partitioning calculation methods



Method 1

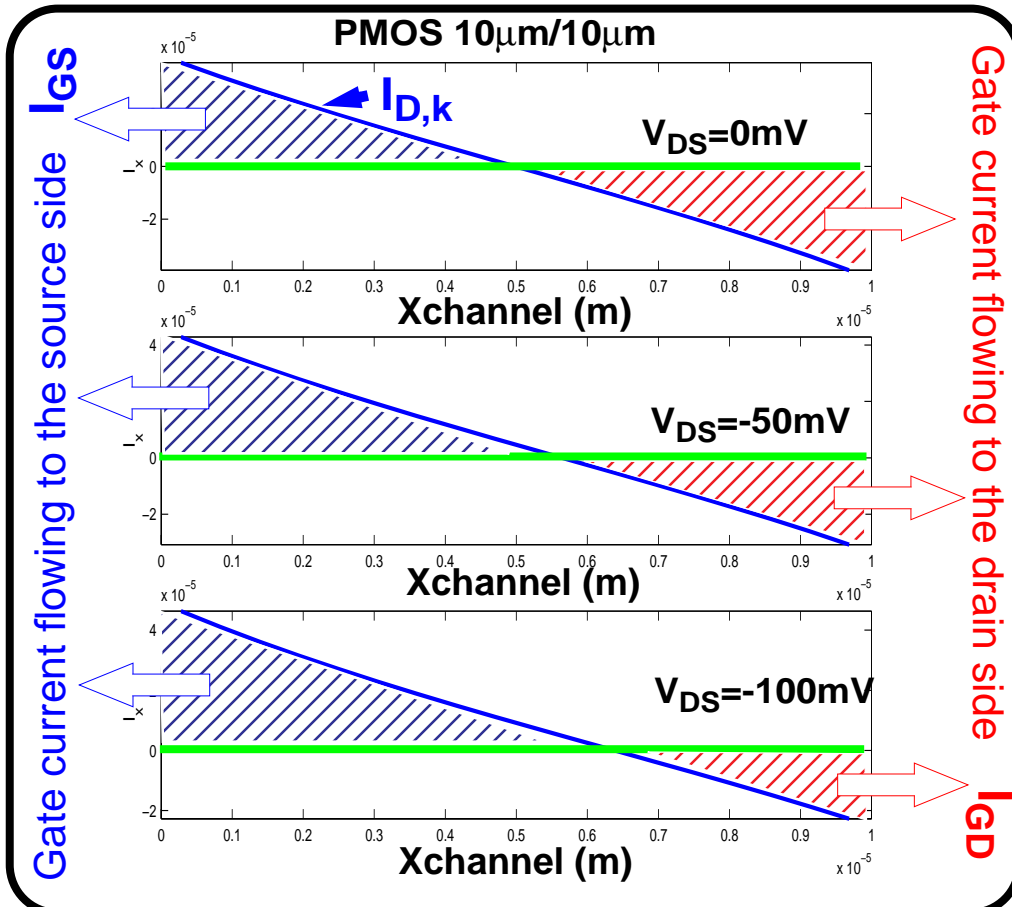
- I_{ch} assumed to be linear along channel

$$\square I_{GS} = \int_0^L \left(1 - \frac{x}{L}\right) \cdot i_G(x) dx$$

$$\square I_{GD} = \int_0^L \frac{x}{L} \cdot i_G(x) dx$$

$$\square \alpha_S = I_{GS}/I_G \quad \square \alpha_D = I_{GD}/I_G$$

Model Application (1/4): Gate current partitioning calculation methods



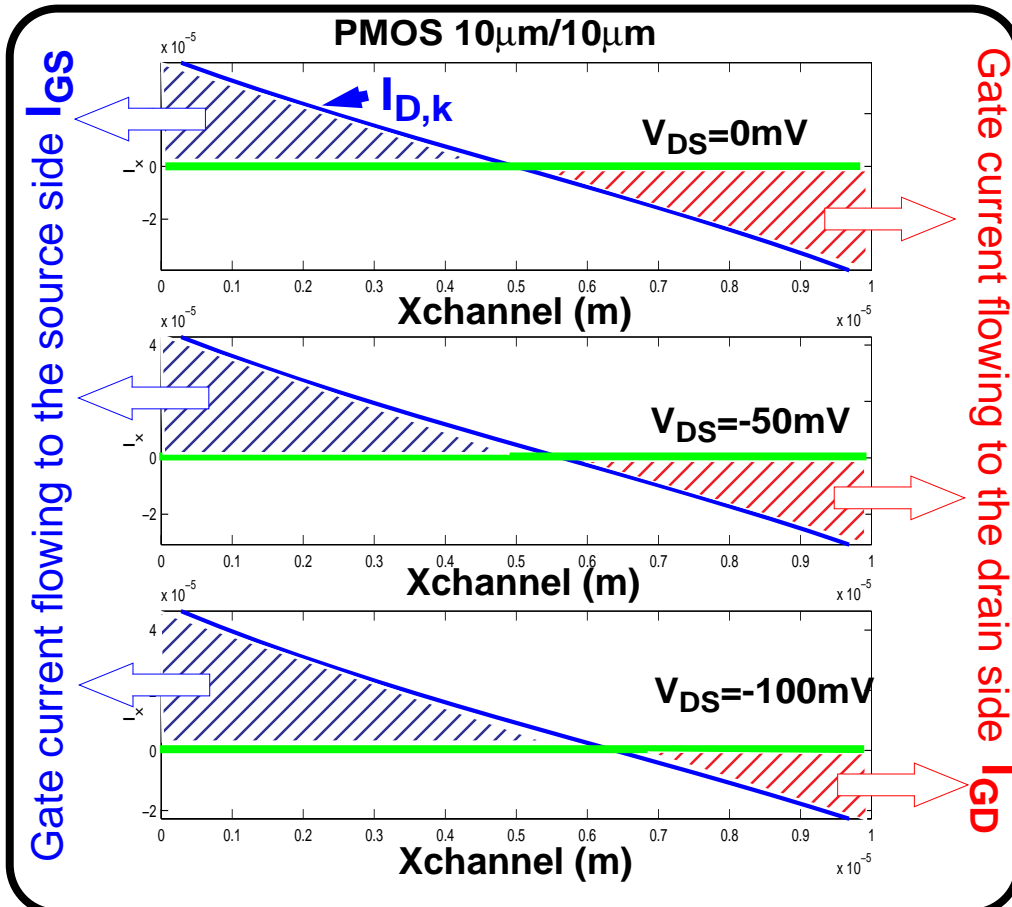
Method 1

- I_{ch} assumed to be linear along channel
- $I_{GS} = \int_0^L \left(1 - \frac{x}{L}\right) \cdot i_G(x) dx$
- $I_{GD} = \int_0^L \frac{x}{L} \cdot i_G(x) dx$
- $\alpha_S = I_{GS}/I_G$ □ $\alpha_D = I_{GD}/I_G$

I_{D0} being intrinsic drain current

→ $\begin{cases} I_{GD} = I_{D0} - I_D \\ I_{GS} = I_S - I_{D0} \end{cases}$

Model Application (1/4): Gate current partitioning calculation methods



I_{D0} being intrinsic drain current

$$\begin{cases} I_{GD} = I_{D0} - I_D \\ I_{GS} = I_S - I_{D0} \end{cases}$$

Method 1

- I_{ch} assumed to be linear along channel
- $$I_{GS} = \int_0^L \left(1 - \frac{x}{L}\right) \cdot i_G(x) dx$$
- $$I_{GD} = \int_0^L \frac{x}{L} \cdot i_G(x) dx$$
- $$\alpha_S = I_{GS} / I_G \quad \alpha_D = I_{GD} / I_G$$

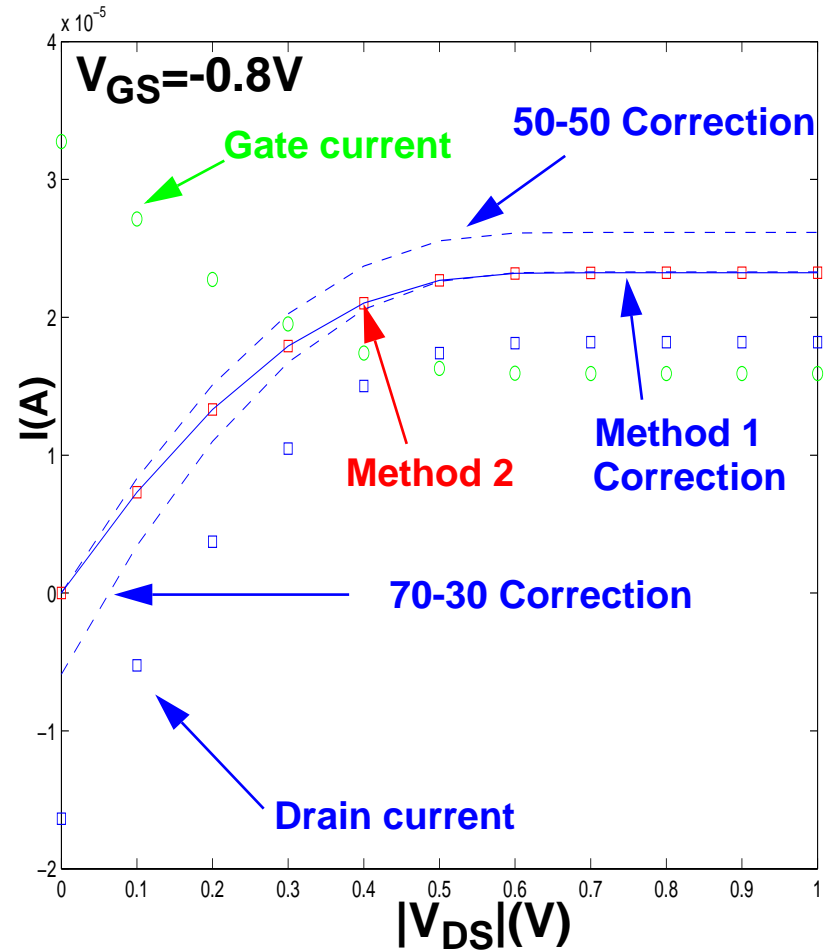
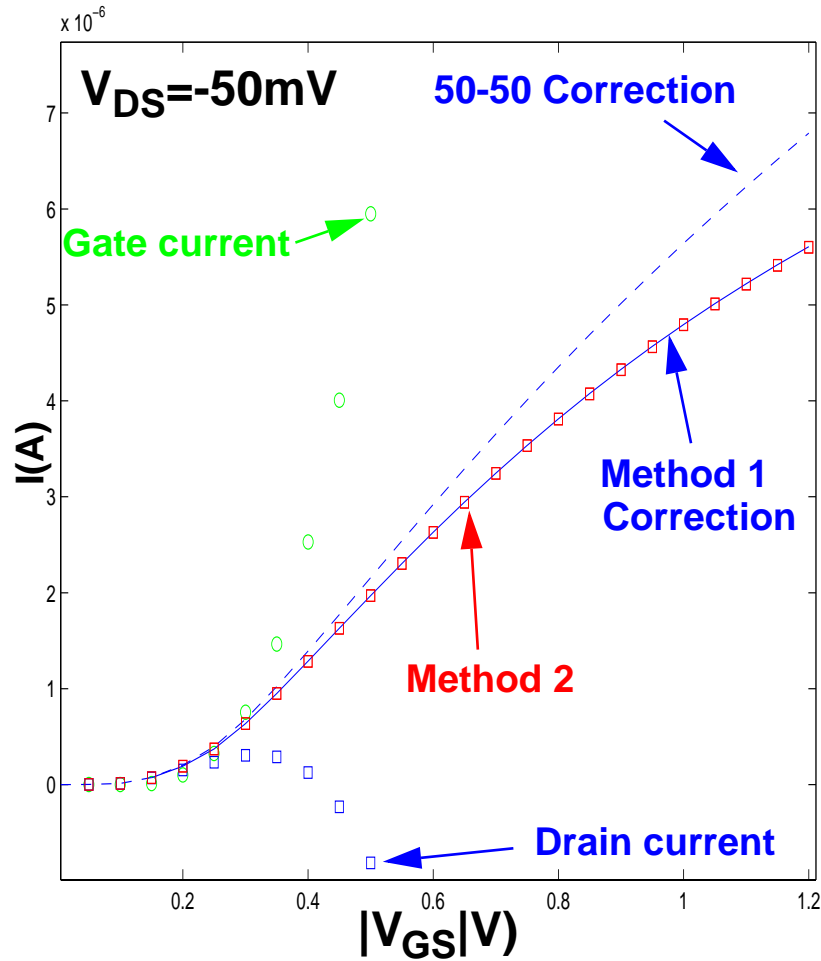
Consistency ?

Method 2

- I_{D0} has to be known
- $$\alpha_S = I_{GS} / I_G \quad \alpha_D = I_{GD} / I_G$$

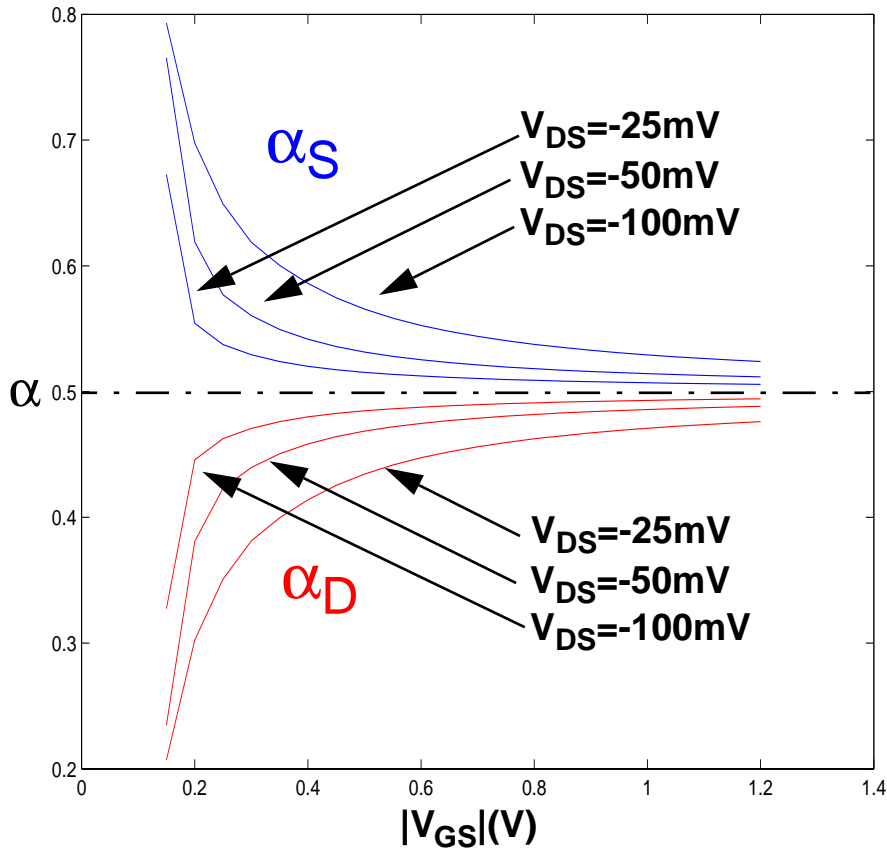
Model Application (2/4): $I_D(V_{DS})$ and $I_D(V_{GS})$ corrections

PMOS $10\mu\text{m}/10\mu\text{m}$ $T_{ox,eff}=13\text{\AA}$

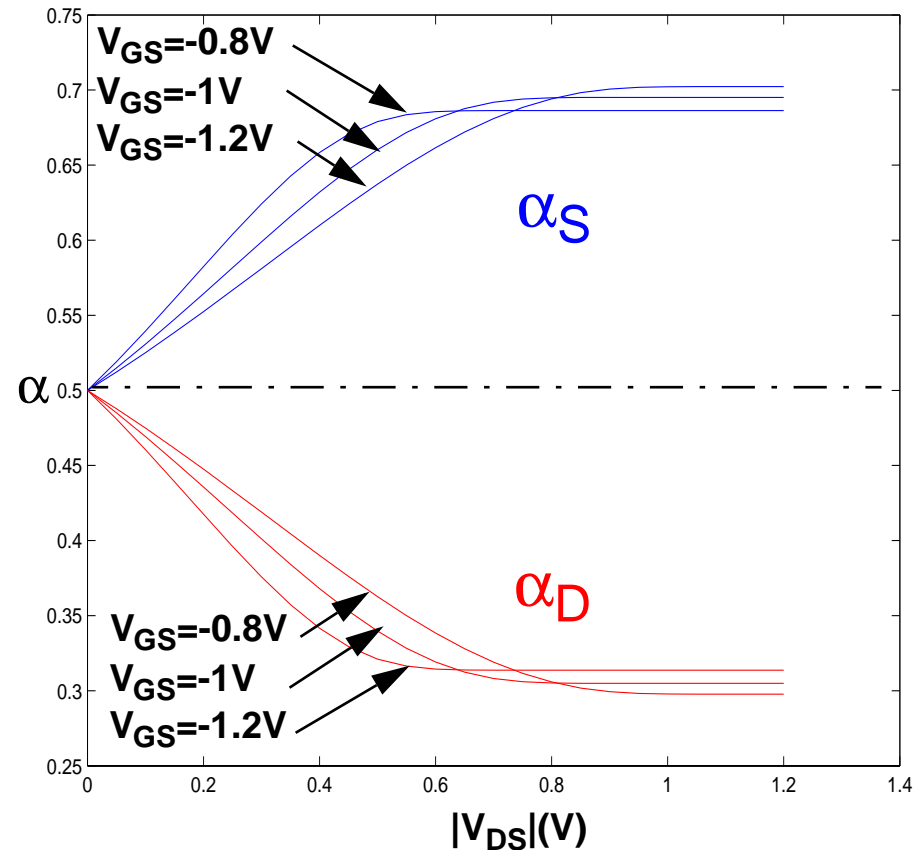


☞ Method 1 consistent with method 2

Model Application (3/4): Partitioning (method 1) vs V_{DS} and V_{GS}

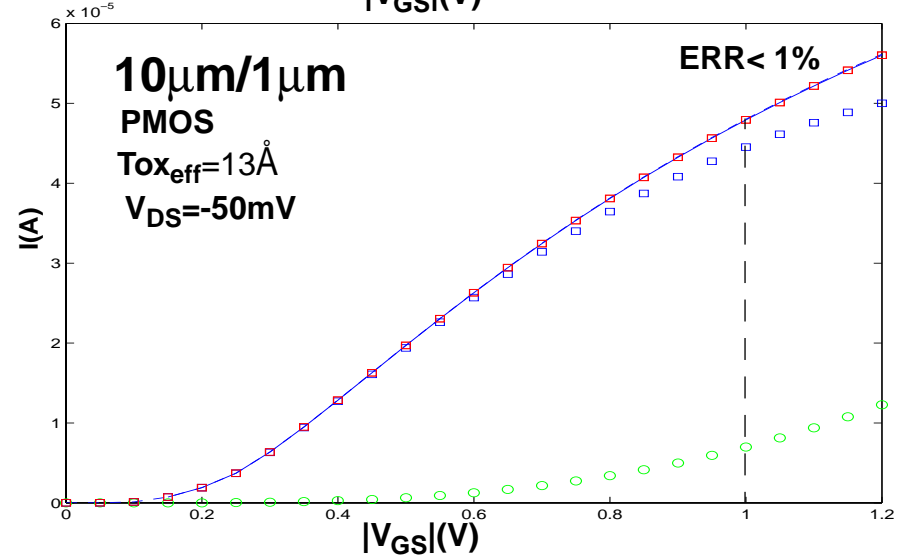
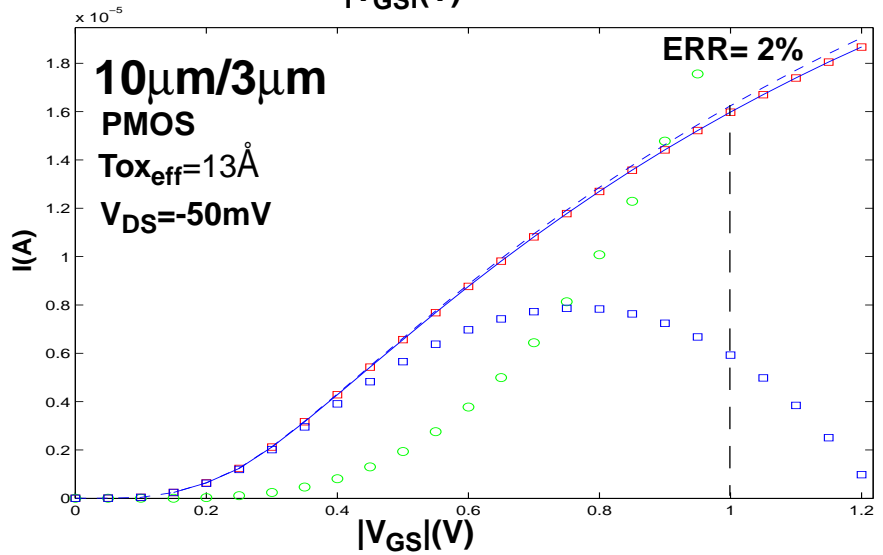
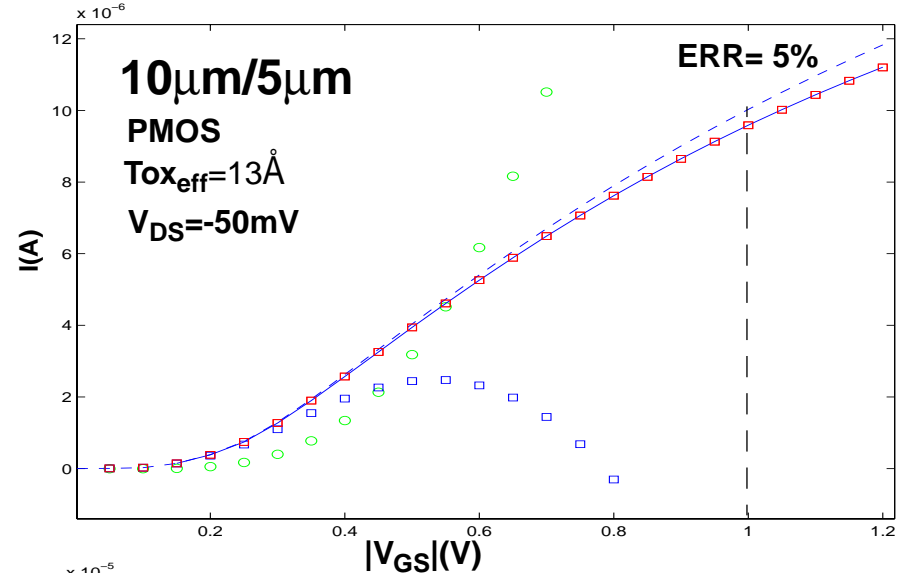
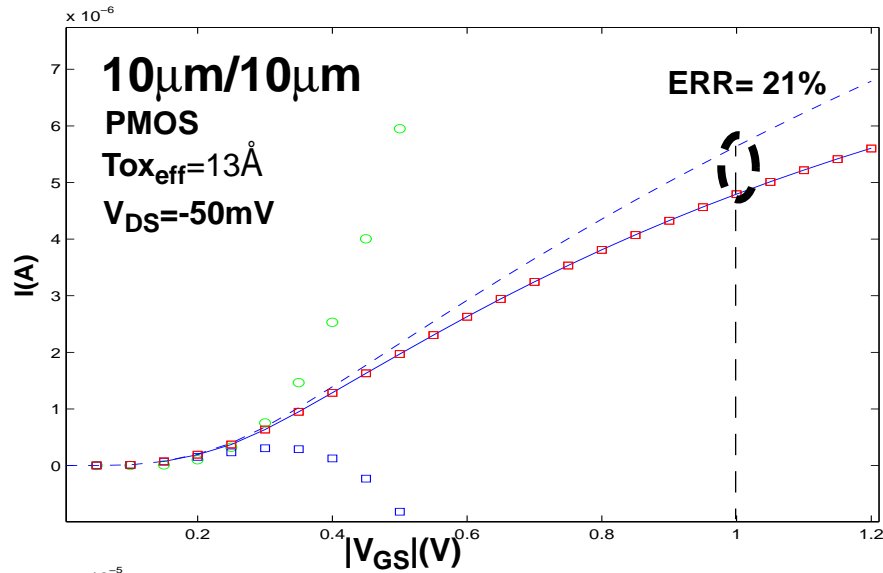


➡ partition far from 50-50 at low V_{GS}



➡ high partition range vs V_{DS}

Model Application (4/4): 50-50 vs accurate correction

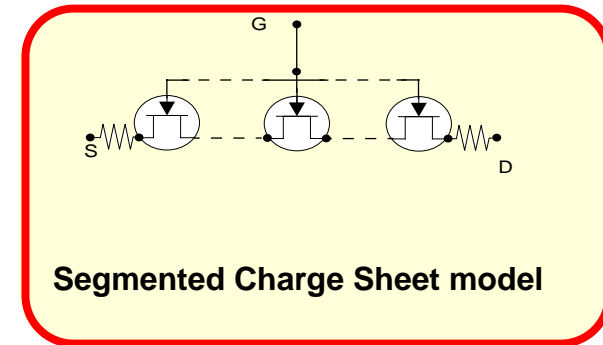
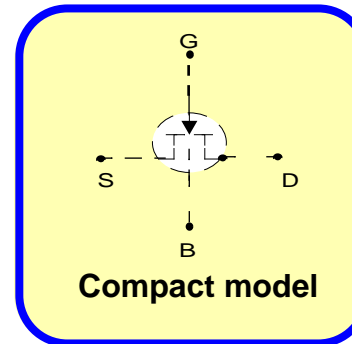


Conclusions For DC modelling on Ultra Thin Oxides

Experiments:

- Strongly debased measured drain current for long channel MOSFETs.
- Area gate current is geometry dependent .

Models:



Solutions for I_G partitioning:

- Segmented MOS model + gate current partitioning integration

- Compact MOS model + $\alpha(V_G, V_D, L, W, T_{ox}, \dots)$ analytical relation..

Solutions for I_G modelling:

- Only segmented model (or equivalent) accounts for channel debiasing