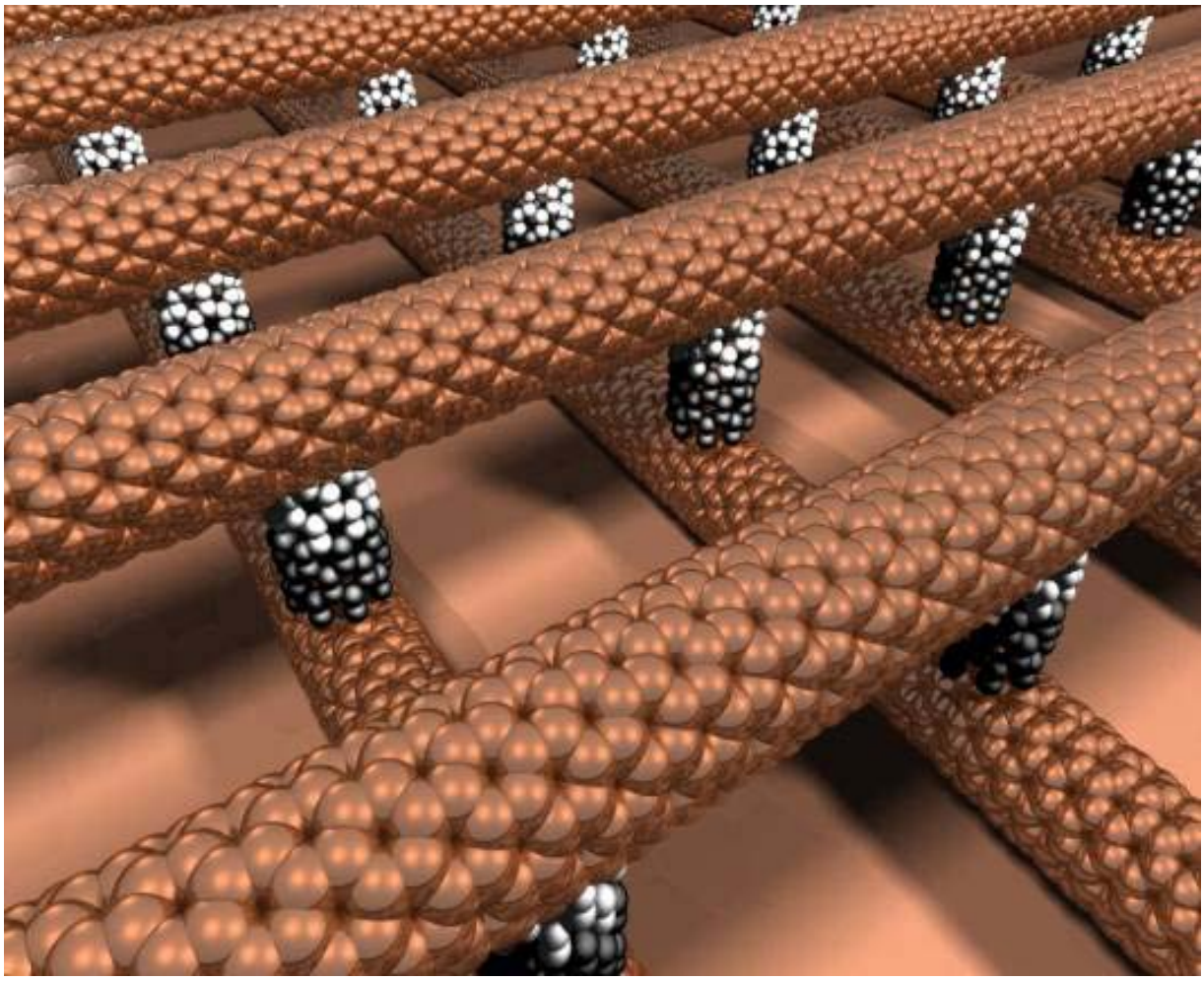
European Nanoelectronics
Initiative Advisory Council

Strategic Research Agenda

Executive Summary



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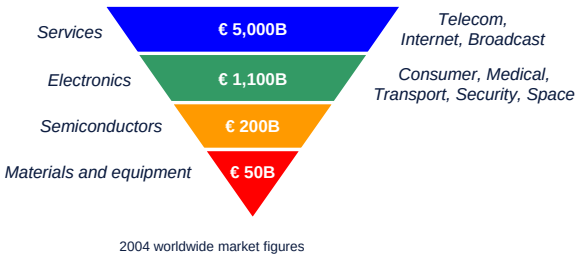
The industrial landscape

Cornerstone of today's and tomorrow's high-tech economy

Microelectronics has pervaded our lives for the past fifty years. Without it, the rich multimedia experience that we have enjoyed from the first days of radio and TV right up to today's world of DVDs, the Internet and computer gaming would not have been possible. Without it, we would not be able to talk to people around the world, exchange text messages or share photographs and video clips via a personal portable device that fits into our top pocket. Without it, our cars would do far fewer kilometres per litre of fuel, heavily pollute the environment and cause more accidents. This massive penetration into consumer, communication and automotive markets means that in 2004 a worldwide 50 billion euro investment in semiconductor materials and equipment led to 200 billion euros worth of semiconductor sales, which were built into 1,100 billion euros worth of electronics equipment, on top of which 5,000 billion euros worth of consumer services were delivered.



Semiconductor technology underpins 5000 billion euros worth of services

The shift from the era of microelectronics, where semiconductor devices are measured in microns (1 millionth of a metre) to the new era of nanoelectronics where they will shrink to dimensions measured in nanometres (1 billionth of a metre) will make electronics even more pervasive than it is today. It will allow much more intelligence and far greater interactivity to be built into many more everyday items around us, with the result that silicon chip technology will play a part in virtually every aspect of our lives – in areas such as personal healthcare, traffic control, privacy and security.

Although Europe has already succeeded in establishing itself as a world leader in microelectronics, it faces formidable challenges in achieving the same world-class position in nanoelectronics. The cost of the research, development and manufacturing infrastructures required will be extremely high and competition from the USA and the Far East will be fierce. However, if Europe is to maintain its position as one of the world's foremost knowledge-based societies, leveraging the potential of nanoelectronics to create highly skilled jobs and economic growth, these are challenges that must be faced.

As silicon solutions become ever more pervasive, the silicon value in products will increase both in terms of hardware and software. The epitome of that today is the mobile phone – almost 100% silicon-based content plus one printed circuit board, a battery and a plastic case. Mobile telephony is already a success story for Europe. The most widely adopted mobile communications standard in the world, GSM (Global System for Mobile Communications), was developed and rolled-out from here.

If the era of microelectronics has achieved all this, the new era of nanoelectronics promises much more. It will not only expand the pervasiveness of silicon solutions, making them small enough, light enough and cheap enough to build into just about anything – even disposable products. It will give next-generation products totally new capabilities that will elevate the ICT (Information and Communication Technology) society to unprecedented levels, and it will enable Europe to realize its vision of Ambient Intelligence – living environments that are aware of our presence and responsive to our needs.European leadership through

The mobile phone – almost 100% silicon-based

R&D ecosystems

Europe already possesses an effective infrastructure for the research, development and production of deep sub-micron semiconductor process technologies. Two of Europe's wafer fabs (Crolles in France and Dresden in Germany) are currently producing 90-nm CMOS devices on 300-mm diameter wafers, which is state-of-the-art in the semiconductor industry. Europe also has some of the world's foremost centres for semiconductor research in the form of IMEC (Belgium), CEA-LETI (France) and Fraunhofer Gesellschaft (Germany).

From a technological point of view this puts Europe in a strong position to realize its visions in the areas of Information and Communication Technology and Ambient Intelligence. Key to this success will be maintaining Europe's world leadership as semiconductor manufacturing moves deeper and deeper into the nanotechnology world, producing silicon chips at the 65-nm, 45-nm and 32-nm CMOS technology nodes and beyond.

Maintaining this leadership will ensure that critical Intellectual Property in the area of nanoelectronics is generated and benefited from in Europe. It will not only create a pool of industrially focused research engineers. It will create highly skilled jobs in the resultant semiconductor, systems integration, product design, product manufacturing and service sectors. In particular, it will further reinforce Europe's existing strength in areas such as telecommunications, medical and automotive electronics.

The prospects for Europe were not always this good. In 1990, only one of Europe's indigenous semiconductor companies ranked in the world's top ten. Worse still, by 1995 none of them did. Yet thanks to the success of the public-private partnerships established in Europe to correct this situation, all three major European semiconductor companies now enjoy a top ten ranking.

The nanoelectronics vision

ENIAC - implementation strategies for a European vision of nanoelectronics

A far-sighted strategy for the European nanoelectronics industry, aimed at securing global leadership, creating competitive products, sustaining high levels of innovation and maintaining top-class skills within the European Union is outlined in 'Vision2020 – Nanoelectronics at the Centre of Change' published by the European Commission. In addition to identifying the technological, economic and societal advantages of establishing Europe as a global leader in nanoelectronics, the 'Vision2020' document clearly highlights the importance of creating effective partnerships in order to achieve this goal.

Europe must not only have access to leading-edge technologies for nanoelectronics. It must also have an efficient means of knowledge transfer between R&D and manufacturing centres in order to turn this technology into leading-edge value-added products and services. Such partnerships will therefore need to include all stakeholders in the value chain, from service providers at one end to research scientists at the other, so that nanoelectronics research can remain strongly application focused.

To create an environment in which these partnerships can flourish, 'Vision2020' proposes the development of a European Technology Platform and a Strategic Research Agenda for nanoelectronics that will enable industry, research establishments, universities, financial organisations, regional and Member State authorities and the EU to interact to provide the resources required, within a visionary programme that fosters collaboration and makes best use of European talent and infrastructures.

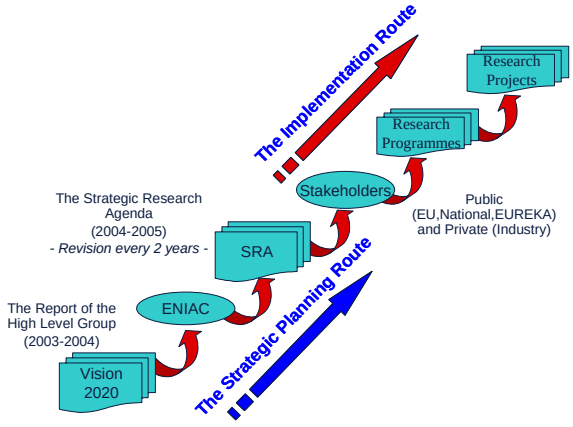
ENIAC (European Nanoelectronics Initiative Advisory Council) has been set up to define and develop this Technology Platform and Strategic Research Agenda.

Nanoelectronics provides underlying technologies for virtually all of Europe's other major technology platforms. Its Strategic Research Agenda, for which this document forms the Executive Summary, details a dynamic strategy for developing the technologies needed to achieve the long-term vision set out in the 'Vision2020' document.

Taking into account the short-, medium- and long-term challenges faced by Europe in realizing its vision of the ICT society and Ambient Intelligence, the Strategic Research Agenda identifies and quantifies the performance parameters needed to measure the progress of nanoelectronics research, development and industrialization. By setting these out as a series of technology roadmaps it will help in the coordination of local, national and EU wide resources – in the form of research, development, manufacturing, educational and regulatory infrastructures – to achieve European success in nanoelectronics. By matching technology push from the scientific community with the innovation of SMEs (Small and Medium-sized Enterprises) and the market pull of large industrial partners and end-users, the Strategic

Research Agenda will ensure that research coordinated under it is industrially, economically and societally relevant. A formal on-going review process will make the agenda adaptive to events such as changing market and societal conditions or the emergence of disruptive technologies.

To generate real economic growth and employment, nanoelectronics research in Europe must be clearly application focused. The Strategic Research Agenda must therefore identify relevant application domains, evaluate future markets in each of them and identify the technological developments needed for market success. It must then define the parameters through which this technological progress can be measured and set out clear parameter roadmaps to direct and evaluate nanoelectronics research.



The Strategic Research Agenda identifies the research and development needed to turn Europe's vision for nanoelectronics into reality

Society needs and technology requirements

Nanoelectronics will provide intelligent solutions to fulfil important societal needs, as exemplified by the following application domains:

Health
'The Doctor in your Pocket'
Real-Time Diagnostics
Bio-Chips / Body-Sensors

Mobility
100% Safety on the Road
Integrated Transport Systems
Prevention of Pollution

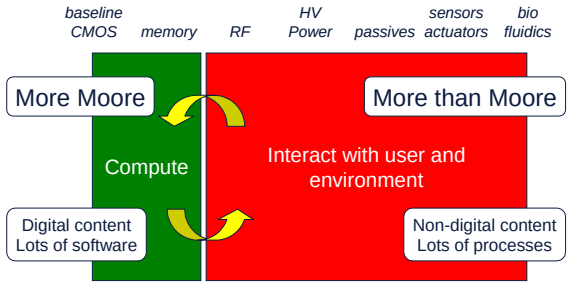
Security
Personal Emergency Systems
Protection against Crime and Terrorism
Secure Home Environment

Communications
Seamless Wired/Wireless Access
Mobile Services without Compromise
Protection of Privacy / Content

Education and Entertainment
Learning Anywhere, Anytime
Content with Best Quality (e.g. HDTV)
Content Protection

Adding intelligence and interactivity to our everyday environment not only means embedding computing power into everything around us – the concept of ubiquitous computing. It also means providing these everyday things with the sensory capabilities and response mechanisms needed to let them interact with human beings and their surroundings – the concept of Ambient Intelligence.

Moore's Law will continue to address the intelligence issue by doubling the computing power that can be put on silicon chips every two years, but what will be needed to implement interactivity will be something considerably 'More than Moore' – technologies that will provide silicon chips with the equivalent of the eyes, ears, arms and legs that allow humans to demonstrate their intelligence in such highly interactive ways.



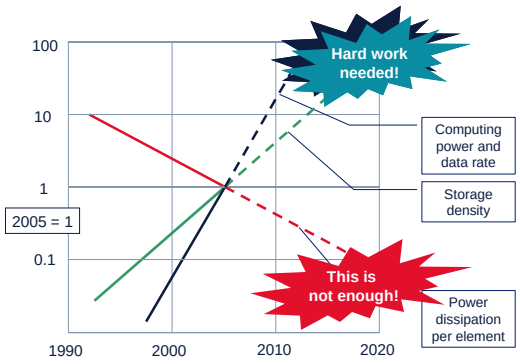
Intelligent systems compute and interact, requiring 'More Moore' plus 'More than Moore'

It will be the combination of nanoelectronics with other nanotechnologies such as nanobiotechnology and nanomechanics that will allow these intelligent interactive systems to be made small enough, cheap enough and sufficiently low power consuming to embed into everyday consumer products.

The performance requirements for these systems can be defined in terms of key parameters, the most important ones being: computing power (Giga-Operations per second), storage capacity (Gbits per chip), data rate (Gbits per second), and power dissipation (nano-Watts per transistor).
In addition to these quantitative measures, there is the increased system functionality that accompanies the growing number of user functions handled by each circuit.

A central characteristic of Ambient Intelligence is that the environment in which we live will be aware of our presence and responsive to our needs. This means that future electronic systems will not only have to have the computing power needed to provide intelligence, they will also require the equivalent of eyes and ears to sense their environment. They will also need the ability to respond to what is going on around them by controlling that environment or by responding to users through human interface modalities such as speech.

Different application domains may differ in the weight given to each of these technological requirements, but nevertheless they are common to all application domains. The Strategic Research Agenda for Nanoelectronics sets out detailed roadmaps for each of these parameters in each of the identified application domains, providing academia and industry with a timeline of clearly defined research and development targets. Cross-correlated, these roadmaps will allow the early identification of technology issues that stand in the way of achieving the required overall system performance in specific application domains.



Differing rates of change for key parameters will lead to technology conflicts that must be resolved

Research priorities

Although research into delivering ‘More Moore’ and ‘More than Moore’ forms a major part of the strategic effort needed to realize Europe’s vision for nanoelectronics, these are not the only areas covered by the Strategic Research Agenda. Underlying both ‘More Moore’ and ‘More than Moore’ there is a large amount of research that needs to be done in materials science and fabrication processes, together with research into disruptive technologies and new device architectures ‘Beyond CMOS’. New assembly and test technologies will need to be developed so that components from all domains can be brought together into total system solutions – so-called Heterogeneous Integration. New extensions of Electronic Design Automation (EDA) tools will be needed that allow designers to implement and verify these solutions from system-level specification down to physical layout in order to ensure short time-to-market and fast ramp-up to volume manufacturing.

Each domain will require strategic direction and roadmaps, together with appropriate consolidated research infrastructures and industry partnerships to achieve its roadmap objectives.

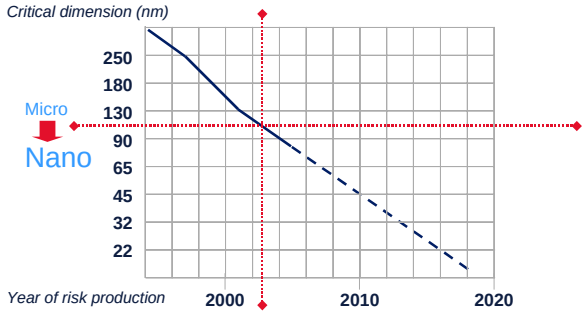
More Moore

CMOS (Complementary Metal-Oxide-Semiconductor) technology has been the key technology driver for microelectronics ever since the beginning of the 'digital era'. Its unique ability to execute binary arithmetic and logic functions (ones and zeros) while consuming extremely little electrical power has made it the technology of choice for digital systems, as used in microprocessors and memories. CMOS is the primary technology specified in the ITRS (International Technology Roadmap for Semiconductors), and will maintain its dominance for many years to come.

The continued predominance of CMOS is due to the success of the semiconductor industry in scaling the size of the transistors on the chip to ever-smaller dimensions. Minimum device dimensions progressed from 10 microns (10 millionths of a metre) in 1970, to around 1 micron by 1988 and to less than 0.1 micron by 2004. Today's figure of 0.1 micron is significant because it is equivalent to 100 nanometres (1000 nanometres = 1 micron), which means that the semiconductor industry has already moved into the realm of nanotechnology. Since its introduction, CMOS has closely followed the bold prediction by Gordon E. Moore in 1965 – commonly known as 'Moore's Law' – of exponential feature-size reduction in the semiconductor industry. The ITRS currently predicts that 32-nm CMOS will be in production by the year 2015.

However, the industrial infrastructure needed to manufacture deep sub-micron chips has become extremely expensive. In Europe, the necessary R&D and manufacturing infrastructures have only been made possible through industry alliances and joint ventures between major industry players. They are the single most important factor in keeping Europe at the forefront of semiconductor R&D and manufacturing. To stay in the race, it is important that the European semiconductor industry continues to invest in its infrastructure so that it can continue to deliver 'More Moore' in-line with the ITRS roadmap.

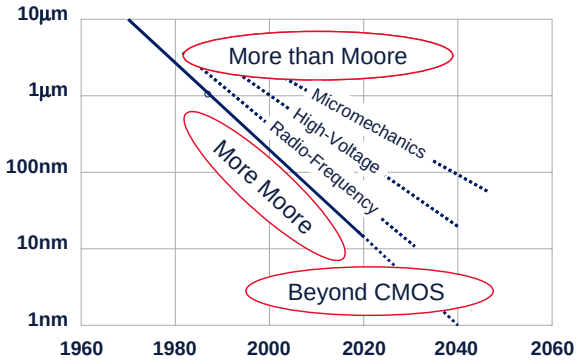
Some of the main challenges include research into new substrate materials and switching devices, the use of non-conventional optical lithography and mask-less lithography, and the integration of nanoelectronics and other innovative devices onto a single substrate.



Europe is at the leading edge of CMOS development

More than Moore

In the world of nanoelectronics ‘More More’ on its own is not enough. What will also be needed is ‘More than Moore’, in the form of functionality enhancing special process technologies that do not scale in accordance with Moore’s Law and cannot therefore be integrated easily in the ‘baseline’ CMOS processes used for state-of-the-art digital logic and memories. Typical examples of ‘More than Moore’ today are the heterogeneous technologies used to implement RF (radio-frequency) active and passive components in wireless transceivers for mobile phones; high-voltage solid-state switches for use in transportation electronics and mains operated circuits, including electronic lighting and battery chargers; and the motion sensors and actuators which are essential elements of car safety systems.



Special semiconductor processes may lag CMOS by several generations but add ‘More than Moore’ to silicon systems

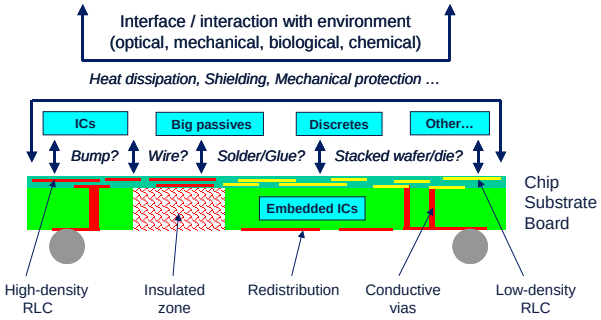
In view of the ongoing demand for performance improvement in a wide range of applications, breakthrough R&D in RF and high-voltage continues to be needed. Other main challenges in the ‘More than Moore’ domain will be to extend the range and diversity of semiconductor processes to allow the implementation of new functionalities, while making the resulting subsystems smaller, lighter, more cost effective and more power efficient. A multitude of heterogeneous technologies for integrating mechanics, fluidics, optics, acoustics, and eventually a direct interface to the human body will be needed to add the full complement of awareness and responsiveness capabilities required for Ambient Intelligence. These nanoelectronic subsystems will form the eyes, ears, arms and legs of Ambient Intelligence – complementing the brains provided by microprocessor and memory subsystems. Possible implementations are integrated solid state cameras, microphones and speakers, solid state lighting, integrated area map and compass modules, or systems to monitor environmental conditions and personal wellbeing and health.

Heterogeneous Integration

In terms of system integration, the ‘More than Moore’ concept might at first seem like a backward step. Instead of achieving a single-chip ‘System-on-Chip’ solution produced in a near baseline CMOS process, systems will once again require the combination of several different chips implemented in different process technologies.

Heterogeneous Integration overcomes this problem by finding ways to integrate all of these separate chips together inside a single package – referred to as a System-in-Package (SiP) – that is no larger than a System-on-Chip (SoC). With a SiP solution, the application benefits from the same level of miniaturization achievable with a SoC but also benefits from having each part of the system fabricated in an optimum process technology. SiP solutions will typically contain SoC solutions (‘More Moore’ solutions) but combine these with other devices that provide better overall value for money (‘More than Moore’ solutions).

Traditionally, device packaging has been a post-fabrication process, performed after the silicon wafer is sliced up into individual chips. The challenge for the nanoelectronics industry will be to find ways of interconnecting these devices at chip-scale levels – for example, bonding one chip directly to another and creating 3-dimensional interconnect structures between them. Another challenge will be the development of wafer-scale packaging technology, in which a protective shell is created around each device as part of the wafer fabrication process. Eventually, process technologies and design environments similar to those used in CMOS today will be needed to meet the manufacturing requirements of Heterogeneous Integration in a cost-effective way.



Heterogeneous integration (SiP) puts multiple technologies into ultra-small packages

Equipment and Materials

Even the extension of existing process technologies into the nanotechnology world will require fundamental research into new materials and methods of production. Getting CMOS to the 45-nm technology node, for example, is already involving research into the use of new materials, such as high-k and low-k dielectrics, that will require significant changes to wafer processing and new equipment installation. Getting it to the 32-nm node will require the installation of a whole new generation of lithography equipment – today's most expensive equipment in a wafer fab.

Combining 'More Moore' and 'More than Moore' devices into total system solutions through the process of heterogeneous integration will also pose challenges both in materials and manufacturing. These challenges include research into new substrate materials and new production techniques in the areas of lithography, thin film deposition and etching, micro-machining, nano-manipulation and metrology. Disruptive technologies such as carbon nanotubes are likely to have an even greater impact on infrastructure investment if they are to reach a production environment.

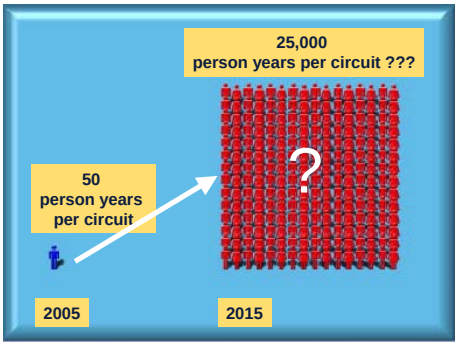
Design Automation

Delivering ‘More Moore’ by keeping pace with the ITRS roadmap and ‘More than Moore’ by extending the functionality that can be integrated, together with solving the challenges associated with Heterogeneous integration, are not the only challenges for success in nanoelectronics. Europe must also address the design gap between what can theoretically be integrated into a SoC or SiP solution and what can practically be designed into it – in other words, the increasing gap between the effectiveness of circuit design and physical circuit density.

Improving design productivity will not be easy in view of the tough requirements imposed by going to ever-finer process geometries, and it will require the adoption of systematic Design-for-Manufacturability (DfM) methodologies. Closing the design gap created by the exponentially growing number of transistors per chip is an even larger problem that can only be solved by raising the level of abstraction to platform-based application design coupled with high-level re-use of hardware building blocks.

Connecting together 1 billion individual transistors into a working system solution is something that can only be done by a computer, but even the latest EDA tools have difficulty in getting it ‘right-first-time’. Yet right first time is in itself vitally important for the industry, because it reduces design costs and minimizes time-to-market, both of which are critical factors in fast-moving electronics markets. Verification on a full virtual SoC/SiP prototype is mandatory to guarantee a fully operational system on first implementation.

SiP technology poses additional design challenges because existing EDA tools are normally dedicated to a single process technology, and by definition a SiP utilizes several different technologies. Designing and simulating SiPs at system-level, which will be the only way of ensuring right-first-time designs, coupled with the need for design for manufacturability, will require many disparate EDA tools to be integrated into a single system-level design environment. With such small package dimensions, even the package characteristics will become part of system-level design, making non-electrical simulation (e.g., thermomechanical) as important as circuit simulation.

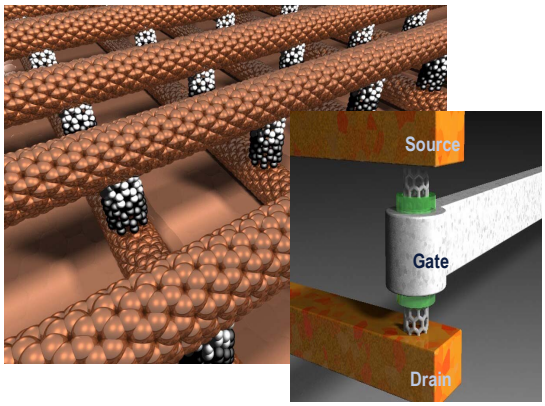


Advanced EDA tools will be needed to maintain short time-to-market for new circuit designs

Beyond CMOS

'More Moore', 'More than Moore', Heterogeneous Integration and Design Automation are central technology pillars that will underpin the future of the nanoelectronics industry for the foreseeable future. In the longer term, however, there will be new disruptive technologies that change the course of events. Beyond the 32-nm CMOS node, for example, innovative nanostructures and architectures will be developed to complement CMOS in enhanced logic implementations.

Examples of this may be the development of new transistors and NEMS (Nano Electro-Mechanical Systems) based on carbon nanotubes, or the implementation of 'spintronics', which utilizes the spin of an electron along with its charge to carry information. And the conventional top-down approach to semiconductor device manufacturing, in which conducting, semiconducting and insulating layers are selectively added and subtracted from a wafer of silicon, will begin to merge with techniques that self assemble these layers analogous to the way that nature builds biological systems.



Disruptive technologies such as carbon nanotubes may change the course of research

Infrastructures and partnerships

Strategic direction

Nanoelectronics is the essential enabler for realization of the vision of Europe set out in 'Vision2020'. However, in order to achieve this objective in the face of mounting competition from other parts of the world, European research into nanoelectronics must remain focused. It must be driven by real society and market needs, replacing yesterday's 'technology push' with an 'application pull' approach that provides continuous feedback to academia and industry on the relevancy and direction of their research.

It should be connected to existing European strengths such as telecommunications, transportation, and medical and it should serve the entire value chain, involving suppliers, producers and users in the process of deciding its strategic direction so that control of every link in the chain remains within Europe. Above all, it must lead to real industrial innovation that serves the economic and societal needs of the European community.

In the pursuit of 'More Moore', Europe already has a world-class R&D infrastructure for advanced CMOS process technology development. This not only includes the required knowledge base, delivered through European centres of excellence and their links with academia, it also includes extensive joint-venture investment in the state-of-the-art wafer fabs needed to develop and industrialize new CMOS processes. The success of this multi-dimensional R&D infrastructure in keeping Europe at the leading edge of the ITRS roadmap for semiconductors has made it an excellent example of 'best-practice' in academic/industrial collaboration.

In order to maintain Europe's world-class position in 'More Moore' research, this R&D infrastructure will continue to need new investment in both capital equipment and human resources. As CMOS feature sizes reach 45 nm and beyond, the need for new lithography techniques and new transistor structures will make research programmes in Equipment and Materials some of the most pressing.
In the areas of 'More than Moore' and Heterogeneous Integration the required competencies are far more diverse than for CMOS. They are, however, considerably less dependent on large capital investment. In these areas the challenge will be to create research networks that will bring together expert knowledge in many different yet equally critical competencies. Much of this expert knowledge already exists in different parts of Europe, but the absence of a binding factor such as the need to access state-of-the-art wafer fabrication facilities has not yet brought it together.

In the same way that European investment in state-of-the-art wafer fabs became a catalyst for cooperation in 'More Moore' research, a catalyst will be needed to unite the players in 'More than Moore' and Heterogeneous Integration. That catalyst must be the realization that European success in nanoelectronics will depend on an accelerated transfer of multi-disciplinary academic knowledge into societally relevant products and services, and an acceptance of the fact that much of that knowledge is located in different industries in different parts of Europe.

The Strategic Research Agenda for Nanoelectronics in Europe therefore needs to be driven by a core group of industrial players and academic institutions that can recognize the challenges involved and pull the necessary resources together. In doing so, it will be able to use many of the best-practice methods already learned from Europe's highly successful 'More Moore' collaborations. However, the research programmes that stem from this agenda will reach much further than those in 'More Moore' research, because many of the competencies needed in nanoelectronics, especially in the areas of 'More than More' and Heterogeneous Integration, lie within the wealth of SMEs at the heart of Europe's economy.

Because many of the devices that will result from research into 'More than More' and Heterogeneous Integration will be based on

silicon wafer processing, Europe's existing semiconductor research ecosystems can act as hubs for knowledge sharing as well as providing shared facilities such as cleanrooms and prototyping equipment. This is already an area where significant private investment is taking place in Europe.

Next to the mandatory improvements to close the design gap in 'More Moore', 'More than More' and Heterogeneous Integration will also open up unique opportunities for Europe's EDA industry as design flows and tools that were originally developed for digital design will need to be redefined and extended to cope with the many different technologies that will go into future nanoelectronic devices. It is not capital investment that is required in this domain. It is investment in creative people and methods of making them more productive.

The 'Beyond CMOS' domain will push the boundaries of scaling to the point where radically new transistor structures or computing architectures will need to be developed. Current research candidates include devices such as carbon nanotube transistors and molecular memories, and it is likely that new 'bottom-up' approaches to device fabrication will have to be combined with traditional 'top-down' technology into a single nanoelectronics manufacturing process. In this domain, even the selection and filtering of ideas in order to extract the main direction for research is a challenge in itself, requiring a great deal of parallel evaluation and structured communication. While the short-term impact may be low, this research must be supported today, otherwise there will be nothing to make a decision about in five to ten years time.

Structures and funding

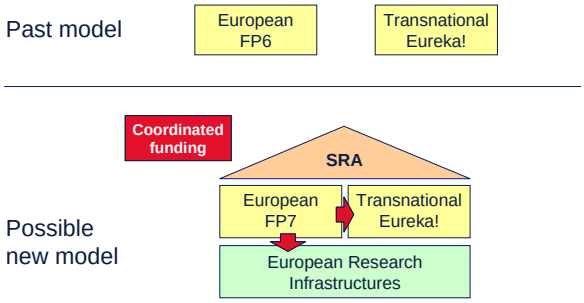
With the worldwide nanoelectronics market growing at some 10% per year, R&D efforts will need to more than double in the coming decade in order to be able to counter the major challenges lying ahead. Apart from the strategic shifts in technical content indicated above, an increasing fraction of the total effort will have to be dedicated to shared technology R&D and precompetitive advanced research, including investments in research infrastructures and pilot lines. Stimulating such cooperative programmes in Europe will make it possible to limit the overall expense associated with product development and production ramp-up, thereby enhancing world-wide competitiveness for the European industry at large.

	2005		2015	
	Private	Public	Private	Public
Advanced research	80	175	140	420
Technology integration	490	325	780	780
Application development	1980	0	3390	0
Prototyping	850	0	1290	0
Million euro per year	**3400**	**500**	**5600**	**1200**

Proposed ENIAC R&D effort sharing through public-private partnerships

Shared R&D efforts through public-private partnerships has proven to be very successful in establishing Europe's position in microelectronics. Extending these partnerships to jointly attack the new challenges of nanoelectronics is the logical way forward. Sharing financing of technology integration on the basis of 50/50 public/private contribution, and advanced research on the basis of 75/25 public/private contribution, is considered a fair overall guide for future programmes. Application development and prototyping are anticipated to be largely covered by private means, as is the case today, which brings the eventual overall percentage of public participation to nanoelectronics R&D to ~18%.

Suitable machinery for creating new European infrastructures and ecosystems for nanoelectronics research already exists in the form of the European Commission's Framework Programme and pan-European EUREKA programmes such as MEDEA+ and PIDEA. Having defined a Strategic Research Agenda for nanoelectronics, the R&D that it identifies as critical to success can be stimulated through these programmes in association with individual member countries. The EC Treaty already includes articles that would allow this coordinated funding to take place between the EU and national R&D programmes.



Proposed model for coordinating European nanoelectronics R&D

Conclusion

Building on existing strengths, the European nanoelectronics industry has the potential to be world-class. The knowledge base, high-skill employment and economic success that it will bring will allow Europe to master its own destiny in the way that it uses information society technologies to fulfil societally relevant needs. As an important part of this endeavour, the ENIAC Strategic Research Agenda will identify key research domains and blocking points and provide guidance for creating the public-private partnerships needed to address and overcome them. It will bring large industrial players, academia and SMEs together into clearly focused ecosystems so that they can jointly face the new challenges, and it will help to create coherent structures for national and pan-European sponsorship to achieve timely results.

Although Europe is in a strong position to make the transition from microelectronics to nanoelectronics, the research challenges and infrastructure investment required should not be underestimated. Europe is not the only part of the world to have recognized the importance of the shift. Nanoelectronics research and development networks are already being established in the USA, Taiwan and Japan, each serving the objectives of their own communities and industries.

This makes it doubly important for all the key players in Europe to work together to ensure the levels of efficiency needed to maintain Europe at the forefront of the nanotechnology revolution. Comprehensively leveraging the knowledge base in Europe is an endeavour that must engage academia and industry alike, bringing together the leading-edge research of universities and research establishments, the specialist knowledge of SMEs and the industrial muscle of large companies to achieve the critical mass needed to achieve breakthrough results. It must be carried out in an environment that promotes the sharing of knowledge and resources in order to achieve common objectives. The cumulative effect will be the creation of a research and manufacturing infrastructure that encourages European nanoelectronics companies to maintain their leading-edge production capabilities, along with the high-skill jobs that go with them, firmly in Europe.

This document was prepared by the ENIAC Working Group SRA on behalf of the ENIAC Steering Committee. The Working Group will extend and detail the Executive Summary into a full Strategic Research Agenda for Nanoelectronics to be presented at the ENIAC Workshop on 16th September 2005 in Grenoble, France. It is foreseen to update the SRA every two years.

More ENIAC information at http://www.cordis.lu/ist/eniac

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