Op-Amp internal circuits
Bipolar (BJT) or MOSFET?

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<th>bip</th>
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<td><strong>Accuracy</strong></td>
<td>+</td>
<td>-</td>
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<tr>
<td><strong>Offset</strong></td>
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<td><strong>Noise</strong></td>
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<td><strong>Process deviation</strong></td>
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<tr>
<td><strong>Chip area</strong></td>
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<td><strong>Voltage capability</strong></td>
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<tr>
<td><strong>Robust at high currents (power)</strong></td>
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<td><strong>Current consumption</strong></td>
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<tr>
<td><strong>Revers-current sensitivity</strong></td>
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<td>+</td>
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N- or P-Input for Op-Amp?

<table>
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<tr>
<th>Condition</th>
<th>Type</th>
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<tr>
<td>min 0 V</td>
<td>pnp, p-channel input</td>
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<tr>
<td>min &lt; 0 (-0.x) V</td>
<td>darlington pnp, p-channel</td>
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<td>min &gt; 0.7V bzw. &gt; Vth</td>
<td>npn, n-channel</td>
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<tr>
<td>max VCC</td>
<td>npn, n-channel</td>
</tr>
<tr>
<td>max &gt; VCC + 0.x V</td>
<td>darlington npn, ..</td>
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\[\Delta = V_{be} \text{ or } V_{th}\]
Comparator, Opamp, OTA?

**Comparator**

The general circuit which is based on a differential-pair input to compare voltages. Output stage can be digital.

**Opamp, Operational Amplifier**

If you use a comparator in a feedback loop, you need a well known frequency response/open loop gain characteristic. You should add internal capacitors which are not required for a comparator.

**OTA , Operational Transconductance Amplifier**

If you take it very seriously, you should say „OTA“ to a simple MOS amplifier because it does not have a high voltage gain, but a high transconductance = ratio of output current / input voltage

MOS-opamp = OTA + output buffer
Comparator, Opamp, OTA?

**Comparator**
- No feedback: high voltage gain, no special frequency response required for stability if no feedback loop
- \[ V_{out} = A \cdot V_{in} \]

**Op-amp** (Operational Amplifier)
- For feedback loop: check frequency response for stability: internal or external frequency components \( (C,R) \) required.
- Output must be able to drive ohmic loads

**OTA** (Operational Transconductance Amplifier)
- Input voltage is translated to output current:
  \[ I_{out} = G_m \cdot V_{in} \]
Basic use of OpAmps

- Noninverting Buffer
- Inverting Buffer
- Noninverting Amplifier
- Inverting Amplifier
Comparator with N-device as input

bipolar: npn-input

MOS: n-channel input

bipolar or MOS: very similar circuit topologies can be used for simple comparators
Simple 1-stage CMOS - OTA

Transconductance: \[ g_m = \frac{I_{OUT}}{(V_{IN1} - V_{IN2})} \]

Current mirror M3/M4 transfers differential input to single output

Recommended rules for transistor sizing:

M1,M2: choose large \( w \) for high gain; large area \( w \cdot l \) for low random offset
M3,M4: choose large \( l \) for high gain and low systematic offset
$g_m$ – compare BJT / MOSFET

**Bipolar:** $g_m$ increases linear with current

\[
I_C = I_S \cdot e^{\frac{V_{BE}}{V_t}}
\]

\[
g_m = \frac{d I_C}{d V_{be}} = \frac{I_C}{V_t}
\]

**MOS:** $g_m$ increases with square root of current

\[
Id = k \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2
\]

\[
g_m = \frac{d Id}{d V_{be}} = k \cdot \frac{W}{L} \cdot 2 \cdot (V_{gs} - V_{th})
\]

\[
g_m = 2 \cdot \sqrt{k \cdot \frac{W}{L} \cdot Id}
\]

bipolar transistor will achieve more $g_m$
2-stage MOSFET – Comparator

Adding a second stage increases the gain and allows full swing at the output

For use as a comparator (without feedback loop): no compensation C required
2-stage MOSFET – OTA „Miller OTA“

For using the 2-stage OTA in a feedback loop add a compensation-capacitor $C_c$ or a compensation network $R + C$
Bode diagram of Miller OTA

1. Without $C_c$: 3 poles created by internal capacitances at nodes A, B, C
2. With $C_c$: set dominant pole to obtain phase-margin

For stability, phase margin $(180° - \phi)$ should be $> 60°$
AC-Simulation of a 2-stage Miller OTA

higher Cc improves the phase margin

$\varphi_m > 45^\circ$ required

> 60° recommended
AC-analysis: Check Stability with Transient Analysis

![Noninverting Buffer Diagram]

- **C = 1/2.5/10/100 pF**
- **with C = 100 fF**
- **without miller-C**
w/l scaling for 2-stage MOSFET - comparator

For MOS comparators/opamps this rule helps to avoid systematic offset, caused by the limited gain of the first stage.

\[(w/l)_1 = (w/l)_2\]
\[(w/l)_3 = (w/l)_4\]

at switching point (V_{IP}=V_{IN}):
\[I_2 = I_3 = \frac{I_1}{2}\]

to avoid systematic offset choose:
\[
\frac{(w/l)_6}{(w/l)_4} = 2 \cdot \frac{(w/l)_7}{(w/l)_5}
\]
How to avoid/to minimize offset of a comparator

Random offset:
Use large devices
Use same size devices for matching, do not match small with large devices
Same orientation
Far away from heating sources (if possible) or on isotherms (line of same temp.)
Symmetric wiring (poly, alu)
Avoid other wiring with high voltages over opamps layout

Use *dummy devices* to improve matching

Try a *centroid layout* for the devices to be matched:
both transistors of a differential pair are
doubled and connected pairwise in parallel
this helps to average out global errors

Systematic offset:
Use symmetry insofar as possible
Most offset is caused by first stages, but do not forget the second stage
Random Offset – Monte Carlo Simulation

for MOS comparators you have to accept an offset in the xx mV range, use MC-simulation to get a better feeling

(simulation done with models of 0.5μm technology with gateoxid = 15nm)

offset simulation:
standard deviation $\sigma = 2$mV, $3\sigma = 6$mV

good centered, no systematic offset
Improve the offset with larger devices.

- $W1, W2 = 100 \mu$m
  - $\sigma = 1.14 \text{ mV}$, $3\sigma = 3.42 \text{ mV}$

- $W1, W2 = 200 \mu$m
  - $\sigma = 0.88 \text{ mV}$, $3\sigma = 2.64 \text{ mV}$

Offset improves approx. with the square-root of the area.
MOSFET - comparator with push-pull current output

Rule for no systematic offset:

\[
\frac{(w/l)_6}{(w/l)_4} = \frac{(w/l)_7 \cdot (w/l)_9}{(w/l)_{10} \cdot (w/l)_3}
\]

The symmetrical design is a method to achieve low systematic offset.

According voltage gain it is rated as a „single-stage“ amplifier, because the output stage is only a current mirror, no gain stage. This low gain also simplifies stability consideration in feedback loops.
MOSFET - comparator (OTA) with cascode output

Cascode output is a method to increase open-loop gain without adding a second stage

Disadvantage: Limited voltage swing at output

VB1, VB2: Bias voltages for cascode
MOSFET - OTA: Folded cascode

static condition: \( I_3 = I_5 = 2 \times I_2 \rightarrow I_6 = I_2, \ I_7 = I_1 \)

Advantage against normal cascode output (page before): extended output swing
Single gain stage, therefore no internal compensation capacitance is required
Folded cascode OTA – frequency response

- Larger $C_{out}$ increases the phase margin.
- No internal compensation-C required.
Folded Cascode example with p-channel input

M58 small compared to M56
- to generate Vcasc only with one transistor

Realized in SPT (BCD) technology
Bipolar (BJT) - comparator

Using bipolar for the main components and MOS for the current sources is a good mix for bicmos opamps and comparators.
Comparator with P-device as input

- Bipolar: npn-input
- MOS: n-channel input

Use P-Input comparators for input voltages near GND (neg. supply voltage)
pnp-input Comparator: Input voltage range
Darlington inputs

pnp - Darlington

P-channel - levelshift

For input voltage range including GND use P-darlington input
pnp darlington comparator: current measurement
**P-input MOS comparator:** logic input buffer with special input specification range
nPN-input comparator: open load voltage measurement
Emitter / Source Follower as Output Stage

Used as buffer.
No voltage gain (=1),
but can deliver
current into a load.

Does not invert the phase,
compared to gain stage

AC: $V_{out} = V_{in}$
DC: $V_{out} = V_{in} - V_{be}$

Signal polarity:

- Emitter follower not inverting
- Gain stage inverting
Opamp as buffer

Vin = Vout -> closed loop gain = 1

For a buffer-circuit with closed loop gain = 1 an amplifier with one gain stage and an output buffer is a good choice to simplify frequency response requirement for stability. Anyway check with AC simulation if compensation C is required.
npn-input Opamp as buffer (voltage follower)

Application: buffer to supply internal bandgap-voltage to a external pin.
Opamp with push-pull output

Application:
Error amplifier in a linear voltage regulator

R,C for frequency compensation
MOSFET - Push-Pull Output Stage

Quiescent current (class A-operation) is defined by:

\[
\frac{(w/l)_4}{(w/l)_2} = \frac{(w/l)_3}{(w/l)_1} = n
\]

\[I_{qu} = n \cdot I_{bias}\]

Similar topology as bipolar push-pull. Current capability not so high caused by significant higher Vgs voltage of MOS compared to bipolar Vbe.
N-input MOSFET comparator with hysteresis

Against the rules here the current mirror transistors M4/M5 has not the same size! This causes an offset and this offset is used to define a hysteresis.

M7 is used as a switch to connect in parallel M6 to M5 if Vout is low.

Resulting offset is larger if gain of comp. is low, therefore w of M1, M2 are small.
nnpn-input, otherwise MOSFET comp.: voltage measurement

Bipolar input for low offset
MOS for smaller area

Unwanted effect of bipolar devices is saturation-behaviour:
Saturation of T2 will increase input current IP.

IN Bicmos designs be careful at the transition points bip–MOS to avoid bipolar saturation effects
Bip/MOSFET Comparator with Hysteresis with clamp voltage (vr3) to avoid bipolar saturation

Q3 clamps Vc of Q2 not to go lower than Vb

vref 1.25V

Adds current in one path to obtain a hysteresis
Calculation of hysteresis of bipolar comparator

If size of M1 not equals size of M2, currents I1, I2 will not be equal. This causes an offset which can be calculated with the $V_{BE}$ equation for bipolar:

$$\Delta V_{BE} = \ln\left(\frac{I_1}{I_2}\right) \cdot V_t$$

Switching on and off this offset depending of the output voltage results in a hysteresis. Hysteresis will be temperature dependent according $V_t$ behaviour.

example for $n=2$: 

![Graph showing Delta VBE vs Temp (C)]
Comparator with emitter-input

nnpn- emitter-input

Note:
Supply current is equal to input currents.
To take into account for accuracy (offset)

For input-range near ground e.g. current measurement
pnp with emitter - input

for input-range near VCC

E.g. current measurement for high side switches
P-channel source-input comparator

Different size of M1, M2 can be used to design a wanted switching threshold Vin > 0
Current measurement with Shunt-Resistor

Requires a reference voltage
Current Measurement with Shunt-Resistor:
emitter-input-comparator, uses $\Delta V_{BE}$ principle

Calculation of threshold $V_S$:

$$V_S = V_T \cdot \ln \left( \frac{n \cdot I_2}{I_1} \right)$$

$n = \text{ratio of emitter areas } Q1/Q2$

e.g. $I_1 = I_2$, $n = 2$  $\rightarrow$  $V_S = 18 \text{ mV} \ @ \ 25\text{C}$

R1 as aluminum-resistor results in a good first order temperature compensation of $V_T$ ($T_{C_{AL}} = 3.8 \times 10^{-3}$)
The layout of the power device (DMOS) in general consists of many cells (> 1000). One or few cells are used as sense cells, the current ratio between main (M1) and sense DMOS (M2) is defined by the ratio $z$. The shunt resistor $R_1$ must therefore not be dimensioned for the full load current and, as an additional advantage, the shunt resistor does not generate a voltage drop in series to the power DMOS.
Current Measurement with Sense-Transistor

Sense-cell with Shunt-Res., Reference-Current with Reference-Resistor

\[ U_{R1} = \left( \frac{I_{\text{Load}}}{z + 1} + I_1 \right) \cdot R_1 \]

with \( I_1 \ll I_{\text{sens}} \) and \( I_1 = I_2 = I_{\text{REF}} \)

the threshold can be calculated:

\[ U_{R2} = I_2 \cdot R_2 \]

\[ I_{\text{OVL}} = I_{\text{REF}} \cdot (z + 1) \cdot \frac{R_2}{R_1} \]

Q1, Q2 are input stages of a comparator and do not use the delta VBE principle!
Current Comparator

A current mirror (bip or MOS) can simply be used to compare two currents.

You can call it a „current amplifier“ or a „current comparator“ where the input signals are not voltages, but currents.
High Voltage Input - Current Comparator with low voltage devices

Only resistors have to withstand the high input voltage (no problem with poly resistors), active devices can be low voltage devices.

MOS-circuit: take care to add z-diodes for overvoltage clamping e.g. against ESD events.
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