Understanding the mobility reduction in MOSFETs featuring high-$\kappa$ dielectrics

P. Toniutti, M. De Michielis, P. Palestri, F. Driussi, D. Esseni and L. Selmi
DIEGM, University of Udine- IU.NET, Via delle Scienze 208, 33100, Udine, Italy,
paolo.toniutti@uniud.it

Abstract

In this paper we analyze by means of accurate Multi-Subband Monte Carlo simulations the mobility reduction associated to high-$\kappa$ dielectrics in a large number of $n$- and $p$-MOSFETs. We argue that soft optical phonon scattering can not explain the experimental mobility reduction for neither the electron nor the hole inversion layer. In order to reproduce the experimental data, a large amount of Coulomb centers in the gate stack is required, which would result in a huge threshold voltage shift not observed in the experiments. Even if we assume the remote charge to be in the form of dipoles, the associated threshold voltage shift is still large and not consistent with the experimental findings.

1. Introduction

The scaling process implies the reduction of the equivalent oxide thickness (EOT) to improve electrostatic integrity and to limit short channel effects. If pure SiO$_2$ is used, oxide thickness below 1 nm is needed in high performance devices scheduled in production for the year 2010 [1]. This results in an excessive gate leakage current due to electron tunneling across the dielectric [2]. High-$\kappa$ (HK) dielectrics can relax this problem since they provide the same EOT with a thicker layer compared to their SiO$_2$ counterpart. Unfortunately, gate stacks featuring HK dielectrics have consistently shown a lower mobility with respect to the well known universal curves. The problem is somewhat alleviated by the introduction of an interfacial SiO$_2$ layer (ITL) between the channel (Si) and the HK material.

Several mechanisms have been invoked to explain this mobility degradation. Soft optical phonons (SOph) have been considered the main responsible for long time, based on the model in [3]. However, more recent studies predict a significantly weaker influence of SOph on the electron mobility [4–6]. Coulomb centers in the the gate stack (remQ) have also been proposed as a possible cause for the mobility reduction [7], but very large charge densities are necessary to justify the experimental mobility degradation [4]. These charges would produce a large flat-band voltage shift inconsistent with the experiments.

Recent experimental data and atomistic simulations suggest that the mobility degradation could be due to interface dipoles close to the HK/ITL interface (DipQ) [8–10]. In the simulation area a large number of models has been proposed which provide quite a broad spectrum of predictions [4, 11], making the global scenario still unclear. In this paper we examine the effect of the soft optical phonons, remote Coulomb scattering and interface dipoles on the $n$- and $p$-MOSFET mobility.

2. Models

We use established Multi Sub-band Monte Carlo (MSMC) models to perform the mobility calculations for electron and hole inversion layers: the model for the $n$-MOSFET is based on the effective mass approximation [12], whereas the one for the $p$-MOSFET [13] is based on the analytical model presented in [14].

In the following, we briefly describe the models implemented to simulate devices with a gate stack featuring an HK sandwiched between an ITL and a metal gate (see Fig. 1). All interfaces are assumed to be abrupt.

A. SOph and remQ scattering

The SOph and RemQ scattering models for $n$-MOS are described in [4]. For the $p$-MOS case, they have been extended using the same formulation for the matrix element, but computing the scattering rate according to the analytical band structure for hole inversion layers in [14].

B. Modelling of the DipQ scattering

On the same grounds as the remQ model [15], the scattering potential due to dipoles oriented perpendicularly to the ITL/HK interface (see Fig. 1) is obtained
by solving the Poisson equation as the sum of the scattering potentials of the single charges constituting the dipole. Clearly, we implicitly assume that the charges belonging to the same dipole (that have different sign) are correlated, whereas the charges belonging to different dipoles are completely uncorrelated. The scattering potential produced in the channel region by a dipole is:

\[ \Phi_{SI}(q, z) = \frac{e}{2\epsilon_{Si}q_{Si}} e^{-q|z-z_{Si}|} \left(1 - e^{-qd_{dip}}\right) + Ae^{-qz} \]  

(1)

where \( e \) is the elementary charge and \( d_{dip} \) is the distance between the charges \( q_1 \) (placed at \( z_{q1} \)) and \( q_2 \) of the dipole (see Fig. 1); \( A \) is a coefficient obtained assuming an ideal metal gate (no scattering potential in this region) and imposing appropriate continuity conditions to the scattering potential and to its first derivative at the interfaces.

3. Simulation results

We now analyze in detail the effect of the SOph, RemQ and DipQ mechanisms on the electron and hole mobility. Please notice that besides the above mentioned scattering mechanisms, peculiar to high-\( \kappa \) dielectrics, the simulations in all the following figures account for acoustic and optical phonons as well as surface roughness and ionized impurity scattering.

A. Effect of SOph scattering

Fig. 2 shows the simulated electron and hole mobility in bulk devices versus the effective field \( (E_{eff}) \) taking into account SOph scattering for various HK dielectrics without ITL. The parameters of the SOph model are taken from [3]. In the \( n \)-MOS case (see Fig. 2a) SOph scattering causes a large mobility reduction, whereas in the \( p \)-MOS case (see Fig. 2b) the effect is negligible, even for HfO\(_2\), which produces the largest mobility reduction in the \( n \)-MOS case. This is due to the much lower phonon and roughness limited mobilities of the \( p \)-MOS compared to the \( n \)-MOS case, which results in a weaker impact of the additional SOph scattering mechanism on the overall mobility.

When simulating a realistic \( n \)-MOSFET, instead, the mobility reduction due to SOph scattering is negligible because it is masked by Coulomb scattering with ionized dopants in the channel and defects at the Si/ITL interface (neglected in Fig. 2) which are instead dominant at low inversion charge and make the total mobility of a realistic device much smaller than in Fig. 2. This has been pointed out in [4] by comparing the simulations to the experiments in [7]. In this work, the trend is confirmed by the simulations of the \( n \)-type devices in [16]. We have first empirically calibrated our simulator on the SiO\(_2\) reference device of [16] (open circles in Fig. 3) by adjusting the charge concentration at the Si/SiO\(_2\) interface and the r.m.s value of the surface roughness, starting from the set of parameters that reproduces the universal curves [17], then SOph for HfO\(_2\) have been activated (filled squares) but results are far from the experimental data for HfO\(_2\) devices.

We have proceeded in a similar way for the \( p \)-MOS case. First, we have calibrated our simulator on the mobility curve of the SiO\(_2\) control device of [7] (open circles in Fig. 4). Then SOph of HfO\(_2\) are activated but Fig.4 shows that the mobility reduction is much smaller than in the experiments for HfO\(_2\) devices.

We have also analyzed SG-SOI \( n \)- and \( p \)-MOS devices to assess if a different electrostatic configuration can change the effect of SOph scattering on the mobility. To this purpose, we have measured SG-SOI MOSFETs fabricated by ST Microelectronics with an undoped 12 nm thick silicon channel. We calibrated the
Fig. 4. Comparison between simulated hole mobility accounting for the SOph mechanism (filled squares), for the SOph and RemQ mechanisms (filled circles) and experimental data (solid line) for the HfO$_2$ devices with $t_{ITL}=1$ nm and $t_{HK}=3$ nm in [7]. The calibration of the model (open circles) with the SiO$_2$ reference device ($t_{SiO_2}=2.5$ nm, dashed line) is also shown ($N_{Si/SiO_2}=5 \times 10^{13}$ cm$^{-2}$, $\Delta_{SR}=0.52$ nm and $\Delta_{SR}=2.0$ nm). The doping of the device is $N_D=2 \times 10^{17}$ cm$^{-3}$.

simulators for $n$- and $p$-MOSFETs on the universal mobility curves of [17] since SiO$_2$ control devices were not available, but the same fabrication process produces bulk devices with mobility close to the universal curves. Fig. 5 compares measurements and simulation results accounting for SOph scattering whose effect is almost negligible, giving a mobility close to the universal curve for both the $n$- and $p$-MOSFETs, whereas the experimental mobility reduction with respect to the universal curves is significant.

B. Effect of the remQ scattering

Fig. 3 shows that to reproduce the experimental reduction of the electron mobility observed in [16], we have to activate the remQ mechanism, assuming a density of charge at the ITL/HK interface $N_{ITL/HK}=4 \times 10^{13}$ cm$^{-2}$ which is very close to that used in [4] to reproduce the $n$-MOS devices with HfO$_2$ of [7].

The hole mobility reduction induced by the HK measured in [7] can be reproduced with the same large charge concentration at the ITL/HK interface (see Fig. 4) necessary in the $n$-MOS devices [4]. Concerning the SG-SOI devices, Fig. 5 shows that a RemQ density of $3 \times 10^{13}$ cm$^{-2}$ and $6 \times 10^{13}$ cm$^{-2}$ is needed in the $n$- and $p$-MOS case, respectively.

By using the RemQ scattering formula reported in Tab. I, the threshold voltage shift $\Delta V_{th}$ produced by remote charges (assumed to be of the same type, i.e. all positive or all negative) needed to reproduce the experimental data of the $n$- and $p$ MOS devices of [7] and for the transistor of [16] are close to 2.22 V and to 0.99 V, respectively. Whereas for the SG-SOI devices of Fig. 5 $\Delta V_{th}$ is close to 0.74 V and 1.48 V for $n$- and $p$-MOS, respectively. These values of $\Delta V_{th}$ are unrealistic and not observed in any experiment.

C. Effect of the DipQ scattering

One would expect dipoles to provide a smaller $\Delta V_{th}$ with respect to the RemQ model. We will see in the following that this is not the case.

Fig. 6 shows the effect of $d_{dip}$ on the simulated electron mobility for dipoles in the $A$-position. The results are in between the case with $d_{dip}=0$ (the effect of one charge is cancelled by the other one) and $d_{dip}=t_{HK}$.

<table>
<thead>
<tr>
<th>Model</th>
<th>$\Delta V_{th}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>remQ</td>
<td>$c \cdot \left[ N_{ITL/HK} \cdot t_{HK} / \epsilon_{HK} \right]$</td>
</tr>
<tr>
<td>A-dipQ</td>
<td>$e \cdot \left[ N_{dip} \cdot d_{dip} / \epsilon_{HK} \right]$</td>
</tr>
<tr>
<td>B-dipQ</td>
<td>$e \cdot \left[ N_{dip} \cdot d_{dip} \cdot (\epsilon_{HK} + 1) / \epsilon_{ITL} \right]$</td>
</tr>
<tr>
<td>C-dipQ</td>
<td>$e \cdot \left[ N_{dip} \cdot d_{dip} \cdot \epsilon_{ITL} / \epsilon_{HK} \right]$</td>
</tr>
</tbody>
</table>

TABLE I

Expressions for the $V_{th}$ shift due to charges of the same sign located at the ITL/HK interface or to dipoles located in the $A$, $B$ or $C$ position (see Fig. 1).
sheet of charge at the Si/ITL interface equivalent to the RemQ model with \( N_{S_i(ITL)} = N_{dp} \). Therefore, for the dipole configurations \( A, B \) and \( C \) in Fig. 1, the densities that reproduce the experimental mobility give a \( \Delta V_{th} \) shift comparable, or even larger, than the RemQ case.

**4. Conclusions**

Multi-subband Monte Carlo simulations suggest that the experimental mobility reduction cannot be attributed to soft optical phonons in either \( n \)- and \( p \)-MOS devices. A huge amount of fixed charges is needed to reproduce the experimental data, but the associated threshold voltage shift (assuming the charges to have the same sign) is very large and inconsistent with the experiments. The situation does not improve if we assume the charge to be in the form of dipoles with dipole moment normal to the ITL/HK interface. Possible models for the remote charge should then assume remote charges with a random distribution of positive and negative charge or dipoles placed parallel to the ITL/HK interface. A recent work ascribes the mobility reduction to neutral defects located at the interface between the channel and the gate stack which are induced by nitrogen diffusion during the fabrication process [18].

Further efforts in the understanding of the possible causes of the mobility reduction are thus necessary.

**Acknowledgments:** Work partly supported by the EU through the NANOsis NoE (IST-216171) and E.C. project GRAND (grant agreement 215752). The authors would like to thank S. Monfray (ST Microelectronics, France) and C. Fenouillet-Beranger (CEA-LETI) for providing the devices in Fig. 5 and C.P. Rossel (IBM, Zurich) for making available the data of [16] in Fig. 3.

**References**