Impact of bias conditions on electrical stress and ionizing radiation effects in Si-based TFETs

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Abstract
The interplay between electrical stress and ionizing radiation effects is experimentally investigated in Si-based Tunnel Field Effect Transistors (TFETs). In particular, the impact of bias conditions on the performance degradation is discussed. We found that the electrical stress effects in TFETs could not be ignored in radiation tests, since they can possibly overwhelm the radiation-induced degradation. Under this circumstance, the worst-case bias condition for studying radiation effects is not straightforward to be determined when there is an interplay between electrical stress and ionizing radiation effects.

1. Introduction
Tunnel Field Effect Transistors (TFETs) are attractive for low power applications, due to the possibility to offer a subthreshold swing (SS) lower than 60 mV/dec [1,2]. The basic TFET structure is similar to a MOSFET except that the source and drain feature the opposite doping types (see Fig. 1(a)). At zero bias, the energy bands are like the solid lines in Fig. 1(b), hence band-to-band tunneling (BTBT) rate is negligible. When TFET is biased to behave as an n-type device (positive drain bias and gate bias), the conduction band of the intrinsic channel region aligns with the valence band of the source region and BTBT occurs.

Recently we have investigated the total ionizing dose (TID) effects in TFETs [3,4]. During irradiation with 10 keV X-ray, we mainly observed a negative shift of the transfer characteristics from the DC test. Meanwhile, an increase in the interface trap density (Nit) was observed from the charge pumping test. Through the comparison of TID vulnerability between conventional MOSFET and TFETs, we observed more severe degradation in MOSFETs and attributed the difference to the particular doping structure of TFETs. Furthermore, the observed degradation of TFETs is due to the charge trapping in the gate oxide [3,4]. When evaluating the radiation vulnerability of conventional MOSFETs, the “worst-case” test scheme is supposed to be implemented in laboratory tests, which corresponds to the strongest radiation-induced degradation and is meant for not overestimating the radiation hardness. For n-channel MOSFETs, the “worst-case” test scheme corresponds to maximize the gate voltage when maintaining other terminals grounded [5].

For devices working under radiation environments, long term reliability has to be considered in addition to radiation vulnerability, since the interplay between the aging process and the radiation effects sometimes cannot be neglected. Combined effects of TID and channel hot carrier degradation have been reported for MOSFETs and BJTs, where evident interplays have been observed [6–8]. Under this circumstance, the evaluation of the real contribution of radiation-induced damage becomes an issue. Therefore, it is necessary to study the interplay between TID and electrical stress.

A similar investigation should be carried out to evaluate the characteristic degradation of TFETs due to both the electrical stress and the ionizing radiation. In this paper, we will present an experimental study of the impact of the bias conditions on the device degradation. A Si-based TFET on SOI structure has been chosen. The results of this work might be difficult to be directly extended to TFETs with different structures and materials, especially to those with different gate dielectrics. However, the concept that the “worst-case” bias scheme for TFETs can be largely influenced by the electrical stress effects is of general applicability.
2. Device and experiment descriptions

Si-based TFETs were fabricated by CEA/LETI, France, using a 100 nm fully depleted SOI process flow. The gate dielectric is a 3 nm HfO2 layer, and additional details on the device processing can be found in [9]. The corresponding \( I_d \) vs \( V_{gs} \) characteristics obtained from DC and pulsed \( I-V \) measurements are shown in Fig. 2(a). For the latter, the trap-assisted tunneling (TAT) contribution is partially suppressed since the gate is pulsed with fast squared pulses [10–12]. The values of SS relative to DC and to the 500 kHz pulsed curves are plotted in Fig. 2(b), showing that in the latter case the minimum value occurs at the lowest measurable current. We can see that the performance of the measured TFETs is modest. According to [9], the drain current of TFETs can be highly improved by means of junction optimization and by replacing the SOI substrate with a SiGeOI structure.

The samples were divided into two groups: the first group was only electrically stressed for \( 10^4 \) s, while the second group underwent a \( 10^4 \) s exposure to a 10 keV X-ray source with a dose rate of 56 rad(SiO2)/s (in this case, both electrical and radiation stresses were applied and the total accumulated dose was 560 krad(SiO2)). During the electrical stress test and the exposure at room temperature, three bias conditions were used separately: (1) \( V_g = 3 \) V, \( V_d = V_s = 0 \) V; (2) \( V_g = V_d = 3 \) V, \( V_s = 0 \) V; (3) \( V_g = 1.5 \) V, \( V_d = V_s = 0 \) V. The stress voltages are significantly higher than the operation voltage of TFETs (the target would be to have TFETs operating at sub-0.5 V) as usually done during accelerated stress measurements. The bias \( V_d = V_s = 0 \) V was chosen considering the possible use of TFETs in circuits like inverters and SRAM cells [13]. In these circuits, n-channel TFETs will operate at \( V_g = V_{dd} \), \( V_d = V_s = 0 \) or \( V_g = 0 \), \( V_d = V_s = V_{dd} \) conditions like nMOSFETs.

The tests were periodically interrupted, then the \( I_{ds} \) vs \( V_{gs} \) characteristics were measured and the charge pumping experiments were performed. To monitor the shift quantitatively, \( V_g \) at \( I_{ds} = 0.2 \) nA/\( \mu \)m is chosen as an indicator of threshold voltage (\( V_{th} \)), as defined in [9]. For the charge pumping test, the gate was driven with a 500 kHz square waveform with 100 ns edge time, 50% pulse duty cycle, 0 V base level and 1.5 V amplitude. The drain and source were maintained at the same potential which was swept from 0 to 2 V [14]. After irradiation, the devices were kept unbiased at room temperature to detect possible annealing effects (i.e. recovery after long time).

3. Results and discussion

In this section, the results of TFETs electrically stressed only are presented and compared first. Then the results corresponding to the three bias conditions under irradiation are presented and discussed.

3.1. Results of TFETs electrically stressed

For the \( V_g = 3 \) V and \( V_d = V_s = 0 \) V biasing, the measured \( I_{ds} \) vs \( V_{gs} \) curves and the charge pumping current (\( I_{cp} \)) of a 10/0.3 \( \mu \)m TFET at different stress times are presented in Fig. 3. From our previous work published in [3,14], the \( V_{th} \) shifts from pulsed \( I-V \) and DC tests are almost the same. So we only analyze results from DC test in this paper. From Fig. 3(a), a shift towards larger \( V_{gs} \) values of the curves is clearly visible. Referring to [14], the degradation is mainly due to the cold electron injection determined by the vertical field component perpendicular to the channel surface. The \( V_{th} \) increase in \( I-V \) measurements indicates the buildup of negative charge in the oxide. This mechanism can be identified also in the charge pumping measurements shown in Fig. 3(b). In the work, the base and top level of \( V_{gs} \) are constant, while \( V_g \) is swept, hence, by
increasing $V_s$, at the same time, we reduce the base and top levels of $V_{gs}$. Accordingly, we see that $I_{cp}$ increases when increasing $V_s$, since the base level of $V_{gs}$ becomes smaller than the flatband voltage ($V_{fb}$). If negative charge trapping occurs in the stressed device, both the $V_{th}$ and $V_{fb}$ increases and, hence, a smaller $V_s$ is required to push the base level of $V_{gs}$ below $V_{fb}$ and to detect $I_{cp}$. Then the left-hand edge of the $I_{cp}$ curve is shifted towards smaller $V_s$. At the same time, it is possible to note how the $I_{cp}$ turn off at around $V_s = 1.6$ V occurs at slightly smaller $V_s$ in the stressed device. This can be related again to a $V_{th}$ increase and, hence, a smaller $V_s$ is required to reduce the top level of $V_{gs}$ below $V_{th}$. Thus the evident shift towards smaller $V_s$ values of the $I_{cp}$ curve of stressed device is consistent with an increase of $V_{th}$ and $V_{fb}$, which are related to negative charge trapping.

From Fig. 3(b), the peak value of charge pumping current $I_{cp,max}$ increases progressively, suggesting an increase in $N_{it}$. The value can be estimated as:

$$N_{it} = \frac{I_{cp,max}}{f \cdot q \cdot A_g}$$

where $f$ is the pulse frequency, $q$ is the unit charge, and $A_g$ is the gate area [15]. From our previous work published in [3,14], the subthreshold slope (SS) characteristics are sensitive to the interface trap density, but the SS can only be observed when the increase in $N_{it}$ is higher than $10^{11}$ cm$^{-2}$, otherwise it will be obscured by the statistical errors. Fig. 4 summarizes the $V_{th}$ shift ($\Delta V_{th}$) and the $N_{it}$ increase ($\Delta N_{it}$) of TFETs electrically stressed under the three bias conditions. Large differences can be observed between the curves. The degradations are more severe under $V_s = 3$ V, $V_d = V_s = 0$ V than under $V_s = V_d = 3$ V, $V_s = 0$ V condition, although the hot electrons are accelerated by the longitudinal field component parallel to the channel direction and injected close to the source/channel junction under the latter condition [16]. Therefore, the performance degradation of TFETs is attributed to the cold electron injection. Fig. 4(a) also shows the average gate leakage density ($J_g$) values during the stress. It can be seen that the higher $J_g$, the stronger the performance degradation of TFETs is. This is consistent with the conclusion above, since $J_g$ is strongly related with the cold electron injection [17].

3.2. Case I: $V_g = 3$ V, $V_d = V_s = 0$ V

Corresponding to the $V_g = 3$ V and $V_d = V_s = 0$ V case, measured transfer characteristics and charge pumping currents before and after irradiation are shown in Fig. 5. The $I_{ds}$–$V_{gs}$ curves shifted to the right after irradiation, i.e., to larger $V_g$ values. Fig. 6 compares $\Delta V_{th}$ of TFET electrically stressed only and the one influenced by the combined effects (i.e., electrical stress plus radiation effects). Negative $\Delta V_{th}$ were expected for radiation induced degradation due to the buildup of positive trapped charge in the gate oxide [3,18], but devices exposed to X-ray with $V_s = 3$ V and $V_d = V_s = 0$ V show positive $V_{th}$ shifts, meaning that, radiation-induced threshold voltage shift were completely compensated by the electrical stress.

The measured $I_{cp}$ (see Fig. 5(b)) continuously increases with the total dose, indicating the progressive increase in $N_{it}$. Fig. 7 presents
the corresponding $V_{th}$ increase, where more interface traps were accumulated in the irradiated TFET than in the one electrically stressed only. From a quantitative point of view, the characteristics shift induced by interface traps $\Delta V_{it}$ can be estimated as:

$$\Delta V_{it} = -\Delta N_{it} \cdot q/C_g \tag{2}$$

where $C_g = 1.58 \times 10^{-6}$ F/cm$^2$ is the capacitance of the gate oxide (the value is provided by the manufacturer). Referring to [19,20], for Hf-oxide devices, the interface traps introduced by TID exhibit the characteristics of positive charge. Thus, the corresponding energy levels should be below midgap and inclined to capture holes.

Table 1 shows the estimated contribution of interface traps to the characteristics shift at the end of exposure/stress, the values are small comparing to the experimental $\Delta V_{th}$. Therefore, radiation-induced interface traps accumulation can be observed, but it is not strong enough to compensate the characteristics shift due to the cold carrier injection induced by electrical stress.

For the irradiated TFET, the $\Delta V_{th}$ values were measured after recovery, and a decrease of about 100 mV could be observed with respect to the end of the stress test. The observed negative $V_{th}$ shift after annealing is now consistent with the radiation effects reported previously [3]. At the same time, after annealing there was an increase in $N_{it}$, which is consistent with the classic theory of TID effects and can be explained by the slow buildup of interface traps [21]. In summary, under this bias condition a sort of interplay between the electrical stress and the radiation-induced charge trapping is found in terms of charge trapping in the oxide.

### 3.3. Case II: $V_g = V_d = 3$ V, $V_s = 0$ V

For the $V_g = V_d = 3$ V and $V_s = 0$ V biasing, the corresponding gate current density during stress is two orders of magnitude lower than in the previous case (see Fig. 4(a)), so the degradation induced by the electrical stress should be highly weakened. Nonetheless, radiation effects were still hidden by the electrical stress since a slight increase in $V_{th}$ has been observed during irradiation in Fig. 8. Consistently with Figs. 7 and 9 show that more interface traps were generated in the gate oxide when both electrical stress and radiation stress were applied. Also under this biasing, the $V_{th}$ shift for the irradiated TFET have been measured after recovery, where a 50 mV decrease was observed. Meanwhile, similarly to the dynamics of $N_{it}$ in Fig. 7, an increase in $N_{it}$ was observed after annealing.

<table>
<thead>
<tr>
<th>$N_{it}$ (cm$^{-2}$)</th>
<th>$\Delta V_{th}$ (mV)</th>
<th>$\Delta V_{th}$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFET irradiated</td>
<td>$1.8 \times 10^{14}$</td>
<td>-18</td>
</tr>
<tr>
<td>TFET electrically stressed only</td>
<td>$1.4 \times 10^{15}$</td>
<td>-1.4</td>
</tr>
</tbody>
</table>
3.4. Case III: $V_g = 1.5\,\text{V}, V_d = V_s = 0\,\text{V}$

In the end, for the $V_g = 1.5\,\text{V}$ and $V_d = V_s = 0\,\text{V}$ bias condition, the gate leakage density during stress is lower than both the previous cases (see Fig. 4(a)). The electrical stress effects were further lowered (becoming negligible), and now the radiation-induced $V_{th}$ decrease was observed during the irradiation procedure (see Fig. 10). After annealing, a partial recover in $\Delta V_{th}$ was observed. Combining the $N_d$ increase (see Fig. 11) of the irradiated TFET with the observed negative $\Delta V_{th}$, this recover in $V_{th}$ is ascribed to the decrease in the radiation-induced positive trapped charge density in the gate oxide. In Fig. 11, the $N_d$ increase induced by the electrical stress was negligible.

Fig. 12 presents $\Delta N_d$ of TFETs exposed to X-ray under the three bias conditions. During irradiation, there were two sources contributing to the measured gate leakage, the gate leakage of TFETs and the photocurrent induced by X-ray exposure. Thus, $J_{g,\text{stress}}$ under the corresponding bias condition is shown in Fig. 12 to illustrate the gate leakage level during irradiation. It can be seen that $\Delta N_d$ of TFETs shows a dependency on $J_{g,\text{stress}}$, indicating that the lower $\Delta N_d$ under $V_g = 1.5\,\text{V}, V_d = V_s = 0\,\text{V}$ is attributed to the lower electric field in the gate oxide during irradiation.

As mentioned before, for n-channel MOSFETs, the worst-case bias condition is thought to be when the gate is applied with the highest operating voltage and other terminals are grounded, since the electric field in the gate oxide is the maximum under this condition [5]. However, in this study, we found that the electrical stress effects in n-channel TFETs could not be ignored and they can even overwhelm and hide the radiation-induced degradation.

Under this circumstance, by using a lower $V_g$ value under which the electrical stress effects could be suppressed, the radiation-induced degradation of $V_{th}$ and $N_d$ can be highlighted.

4. Conclusion

The combined effects of electrical stress and ionizing radiation were investigated in Si-based TFETs. Three bias conditions were chosen, then the comparison of performance degradations was discussed between TFETs electrically stressed only and those subject to both effects. We found that when $V_g$ was large and the electrical
stress effects were noticeable, the radiation effects were obscured by the degradation induced by electrical stress. In particular, the negative shifts of $V_{th}$ typical of the radiation-induced degradation only got revealed after recovery. Under this circumstance, the worst-case bias condition for studying radiation effects is not straightforward to be determined when there is an interplay between electrical stress and ionizing radiation effects.

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References