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On the electron mobility enhancement in biaxially strained Si MOSFETs

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Abstract

This paper reports a detailed experimental and simulation study of the electron mobility enhancement induced by the biaxial strain in (001) silicon MOSFETs. To this purpose, ad hoc test structures have been fabricated on strained Si films grown on different SiGe virtual substrates and the effective mobility of the electrons has been extracted. To interpret the experimental results, we performed simulations using numerical solutions of Schroedinger–Poisson equations to calculate the charge and the momentum relaxation time approximation to calculate the mobility.

The mobility enhancement with respect to the unstrained Si device has been analyzed as a function of the Ge content of SiGe substrates and of the operation temperature.

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1. Introduction

High mobility channel materials for MOSFETs can possibly improve the speed of VLSI–ULSI circuits independently of the geometric scaling of the gate length and gate dielectric thickness. Therefore, the fabrication of strained Si channels with high values of the electron and hole mobilities has gained remarkable interest for high performance CMOS technology [1].

The epitaxial growth of thin Si films on top of relaxed SiGe substrates induces a biaxial strain in the lattice structure of crystalline silicon that splits the 6-fold degenerate valleys of Si into the two sets of the 2-fold and the 4-fold bands, respectively, and leads to negligible modification of the effective masses. This energy splitting depends on the strain/stress level, hence on the Ge content of the underlying relaxed SiGe substrate and, in turn, it increases the population of the 2-fold valleys at lower energy and it reduces the intervalley phonon scattering [2]. Since the 2-fold valleys have a smaller in-plane effective mass than the 4-folds ones, an enhancement of the electron effective mobility ($\mu_{eff}$) in strained Si MOSFETs is observed with respect to unstrained silicon devices [3–6]. Moreover, since the effect of strain on the fraction of electrons placed in the lower 2-fold valleys and on the intervalley transitions depends on the value of the induced energy splitting, the mobility enhancement in strained silicon (sSi) directly depends on the Ge content ($x$) of the underlying Si$_{1-x}$Ge$_x$ layer [7]. The physical mechanisms yielding this mobility enhancement are, however, not clearly understood yet.
In this framework, this paper presents a complete characterization of the mobility in nMOS strained Si devices carried out to investigate its dependence on the level of strain in the channel and on the operation temperature. The experimental results are compared with simulations performed with state of the art numerical models to attempt the interpretation of the experimental data and to gain insight on the physical mechanisms responsible for the electron mobility improvement.

2. Device fabrication and mobility extraction procedure

To study the influence of the strain level on the mobility enhancement, two lots of wafers with long channel MOSFETs have been fabricated having sSi layers with different as-grown thickness ($T_{sSi}$ = 10, 13 and 18 nm) on top of thick relaxed Si$_{1-x}$Ge$_x$ virtual substrates (the subsequent oxidation used to form the gate dielectric reduces $T_{sSi}$ of about 3 nm). The relaxed Si$_{1-x}$Ge$_x$ layer features a Ge content $x$ ranging from 0.15 to 0.27 and was formed by CVD on top of graded buffer layers. Reference devices featuring an epitaxial unstrained silicon channel have been also fabricated. In all samples, the thermal gate oxide is 2.8 nm thick (extracted by ellipsometry) and the 150 nm thick n+ poly-Si gate is in-situ Phosphorous doped with a concentration of about 3x10$^{20}$ cm$^{-3}$ (extracted evaluating the poly depletion effect in the CV measurements).

To get rid of the possible effect of the source and drain series resistances on the I–V measurements, we designed special MOSFET structures with Kelvin probes similar to those of [8] (Fig. 1, upper part), in order to extract the intrinsic conductance of the channel $g_D$. More precisely, by using the internal voltage probes $V_{DI}$ and $V_{SI}$ we have determined the intrinsic conductance as [8]:

$$g_D = \frac{I_D}{V_{DI} - V_{SI}} \frac{L_{int}}{W}$$  \hspace{1cm} (1)

where $I_D$ is the drain-to-source current, $W$ is the device width and $L_{int}$ is the distance between the internal voltage probes.

The inversion charge per unit area $Q_{inv}$ is obtained by integrating the gate-to-channel capacitance $C_{GC}$ given by the split capacitance-voltage (CV) measurements as a function of the gate voltage $V_G$. Thus, the inversion charge density $Q_{inv}$ is readily given by:

$$Q_{inv}(V_G) = qN_{inv} = \frac{1}{W} \int_{–\infty}^{V_G} C_{GC}(V'_G)dV'_G$$  \hspace{1cm} (2)

where $N_{inv}$ is the electron density per unit area of the inversion layer and $(W \cdot L)$ is the total device area. We explicitly verified that thanks to the relatively thick gate oxide, gate leakage has negligible impact on the extracted charge and intrinsic conductance, even in the largest test structure. Finally the effective mobility is calculated as a function of $g_D$ and $Q_{inv}$ [8]:

$$\mu_{eff} = \frac{g_D}{Q_{inv}}$$  \hspace{1cm} (3)

Fig. 1 (lower part) reports the extracted $\mu_{eff}$ as a function of the surface electron density $N_{inv}$ obtained from mobility structures with different lengths and widths (open symbols). We see how the measurements exploiting the Kelvin probes give very similar $\mu_{eff}$ up to high $N_{inv}$ values for all devices, independently of possible series resistances. Moreover, Fig. 1 shows how the series resistance degrades the $\mu_{eff}$ values extracted from a MOSFET with no internal voltage probes (filled symbols), where the channel conductance has to be evaluated from the external drain-to-source voltage drop.

3. Experimental results

For each fabricated sample, we carried out $I_D$–$V_G$ and CV measurements in order to obtain $g_D$ and $Q_{inv}$ and to calculate the electron mobility with Eq. (3). A summary of the results is given in Fig. 2, which shows the $\mu_{eff}$ values versus the effective vertical field $E_{eff}$ extracted from the mobility structures featuring sSi grown on top of substrates with Ge content of 15%, 20% and 27% (open symbols) and from the reference unstrained device (filled symbols). The effective field in the channel is calculated as a function of the inversion charge density according to [11]:
\[ E_{\text{eff}} = \frac{1}{\varepsilon_{\text{Si}}} \left( Q_d + \frac{1}{2} Q_{\text{inv}} \right) \]

where \( \varepsilon_{\text{Si}} \) is the permittivity of Si and \( Q_d \) is the depletion charge per unit area. This latter quantity has been evaluated from the doping profile provided by the process simulations. Moreover, we took into account the fact that the depletion region extends into the SiGe layer, where the permittivity is greater with respect to Si and it has been estimated as a linear interpolation between the silicon and germanium permittivities as a function of the Ge mole fraction.

The electron mobility of the unstrained Si device (Fig. 2, filled symbols) agrees well with data for reference unstrained samples reported in literature (lines) [3–5]. Our data cover a broad range of \( E_{\text{eff}} \) values, nicely bridging previously published results. The sSi structures present a large mobility improvement with respect to the reference Si, with an increasing \( \mu_{\text{eff}} \) for increasing Ge content in the substrate (open symbols). Moreover, we observe that for the same percentage of Ge in the substrate, the extracted \( \mu_{\text{eff}} \) is the same for devices with 10 and 13 nm as grown \( T_{\text{Si}} \) (corresponding to approximately 7 and 10 nm final \( T_{\text{Si}} \) after processing). As it can be seen, also the sSi data are in good agreement with mobility values reported in previous works for devices with similar level of strain in the silicon channel (lines) [3–5], thus proving the quality of the samples and the dependability of the obtained mobility curves.

In order to better understand the mechanisms responsible for the mobility enhancement, we characterized the electron mobility of strained devices at different operating temperatures (\( T \)) and, as shown in Fig. 3, our experimental results agree very well with published data for similar devices in a large range of temperatures. This comparison confirms, ones again, the quality of the fabricated samples.

From Fig. 2, it is possible to evaluate the mobility improvement due to strain by defining the mobility enhancement factor (EF) as the ratio between the extracted mobility of strained and unstrained silicon [3]:

\[ \text{EF} = \frac{\mu_{\text{eff}}^{\text{sSi}}}{\mu_{\text{eff}}^{\text{Si}}} \]

The results are plotted in Fig. 4, where it is possible to observe how EF monotonically increases with increasing Ge content in the substrate. Moreover, for a given sSi device, hence for a fixed strain level in the channel, the enhancement factor is approximately independent of \( N_{\text{inv}} \), hence it is the same for both medium and large \( E_{\text{eff}} \) values [1].

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No saturation effect is seen in our data \[3\].

Enhancement Factor

\[ \mu_{\text{eff}} \] dominates the electron mobility. This results in similar \( \mu_{\text{eff}} \) in the weak inversion region for the strained and unstrained samples at very low \( T \).

At large \( E_{\text{eff}} \) (open symbols), where \( \mu_{\text{eff}} \) is dominated by the surface roughness (SR), the reduction of the enhancement factor with decreasing \( T \) is weaker, but still appreciable, in agreement with data recently reported in \[12\]. At the moment, both the large mobility values and the temperature dependence of the \( \mu_{\text{eff}} \) dominated by SR are not well understood \[13,14\] and, in order to help interpret this reduction of the EF at different \( E_{\text{eff}} \), we performed numerical simulations of mobility in sSi.

In order to gain insight into the mobility enhancement of strained Si channels, we fully characterized the \( \mu_{\text{eff}} \) of our devices over a wide range of operating temperatures. Fig. 6 shows the \( \mu_{\text{eff}} \) curves for the sSi device with a Ge mole fraction of 27\% and for the unstrained Si at a temperature ranging from 425 K to 77 K. For both devices the mobility is increased at low temperatures, because of the reduction of phonon scattering \[11\]. From the measured \( \mu_{\text{eff}} \) we calculated the EF values for different operating temperatures and Fig. 7 reports the enhancement factors obtained for medium and large \( E_{\text{eff}} \) as a function of \( T \). These \( E_{\text{eff}} \) values roughly correspond to the phonon scattering limited and surface roughness limited mobility regimes. Despite an almost constant EF for temperatures larger than 200 K, for very low \( T \) we observe a significant decrease in the mobility enhancement at both \( E_{\text{eff}} \) values. At a medium \( E_{\text{eff}} \) of 0.6 MV/cm (filled symbols), there is a strong reduction of the enhancement factor, in agreement with the data reported in \[3\], which were measured at the mobility peak, hence at an \( E_{\text{eff}} \) not far from from 0.6 MV/cm (see Fig. 2). This is probably due to the fact that the channel quantization is known to produce an energy splitting between the 2-fold and 4-fold valleys that, at very low \( T \), is large enough to place almost the entire inversion charge in the 2-fold lowest subband. Furthermore, at low temperatures, the number of phonons able to assist the intervalley transitions is drastically reduced, according to the Bose–Einstein Statistics. Therefore, in this range of temperatures, the further energy splitting of valleys induced by the strain of the silicon lattice is less beneficial for the electron mobility. This results in similar \( \mu_{\text{eff}} \) in the weak inversion region for the strained and unstrained samples at very low \( T \).

Fig. 5 reports the EF versus the Ge content and we see how the enhancement factor increases with increasing Ge content in the substrate, hence increasing the strain in the channel \[9\]. In particular, we found a proportionality between the EF and the Ge percentage and, thus, between the \( \mu_{\text{eff}} \) increase and the strain level. As predicted by Fig. 4, the same EF dependence holds for both medium and large effective normal fields \( E_{\text{eff}} \). Our results agree with those showed in \[5\] and \[10\] and, in particular, they do not show a saturation of the enhancement factor as reported in \[3\] and predicted by the numerical simulations of \[2\].

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4. Mobility simulations

We calculated $\mu_{\text{eff}}$ in strained Si devices using the model of [16], that is based on the momentum relaxation time (MRT) approximation. The MRT is known to provide accurate results in agreement with more complex Monte Carlo calculations in the limit of small lateral electric field. The subband energies and the wavefunctions are calculated with a one-dimensional, self-consistent Schroedinger–Poisson solver [15], that assumes a close boundary condition for the solution of the Schroedinger equation, hence neglects the wavefunction penetration in the gate oxide. Moreover, since the inversion layer is totally confined in the strain Si film, in the simulations we considered only the strained silicon layer.

Fig. 8 (left plot) shows the comparison between the measured CV characteristic of the unstrained Si device and the simulation performed with the Schroedinger–Poisson solver. In this simulation we used the doping profile provided by the process simulations (Fig. 8, right plot) and we took into account the band-gap narrowing and the work-function shift due to the very large poly doping concentration [17]. As it can be seen in Fig. 8 (left plot), good agreement between the measurement and the simulation is obtained with no further adjustment of the parameters.

First, the mobility model was calibrated by means of the comparison with the universal mobility curves for unstrained silicon [11]. In the simulations (Fig. 9) the phonon scattering includes both the intravalley transitions assisted by acoustic phonons and the intervalley transitions [16]. Moreover, we used either the parameters for the phonon scattering reported in [18] or those proposed in [2]1, that have been summarized in Table 1. For the surface roughness (SR) scattering, we used the Ando’s model [19] and the parameters reported in [20], hence a r.m.s. value of the SR spectrum of $\Delta = 0.62$ nm. With both sets of parameters for phonon scattering, simulations (symbols) agree quite well with the experimental data (dashed lines) over a wide range of temperatures. The experimental curves of our reference unstrained device (Fig. 9, solid lines) indicate that the mobility at small $N_{\text{inv}}$ is slightly degraded with respect to the data of [11] (dashed lines), probably because of a non-optimal silicidation process of the source and drain diffusion in proximity of the transition to the channel during the fabrication of the first lot of wafers. However, this slightly reduced mobility at low $E_{\text{eff}}$ does not influence the extracted EF values. In fact, in that region, the strained Si devices present similar roll-off in the mobility curve (Fig. 2) and the calculated mobility enhancements are in close agreement with those observed in [10] (see Fig. 5), where the reference unstrained device shows mobility values in close agreement with the universal mobility curve [11]. In the following the EF values reported

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1 After private communication with the authors, phonons parameter have been corrected with respect to those reported in [2].
in this work are extracted for $E_{\text{eff}}$ values large enough to avoid any possible effect of the roll-off in the mobility curves.

Fig. 10 reports the experimental and simulated mobility curves for the strained device with Ge content of 27% (open symbols) and for the unstrained silicon (filled symbols). To reproduce the experimental curves, the solution of the Schrödinger equation takes into account the additional valley splitting due to strain, calculated as a function of the Ge mole fraction $x$ [21,20]:

$$\Delta E = 0.67x \quad [\text{eV}]$$

We see (open squares) that, if we keep the same SR spectrum parameter $\Delta = 0.62$ nm used to fit the unstrained mobility curve (Fig. 9), the simulations of $\mu_{\text{eff}}$ in strained silicon show a modest mobility enhancement in the medium $E_{\text{eff}}$ range, while essentially no mobility improvement is seen at large $E_{\text{eff}}$. The simulated mobility enhancement is much smaller than it is observed in the experiments throughout the whole $E_{\text{eff}}$ range (open and filled circles) [20] with both the phonon scattering parameters proposed in [18] (solid lines) and the corrected set of Table 1 derived from those of [2] (dashed lines).

In the attempt to reproduce the sSi mobility, especially at high $E_{\text{eff}}$, we followed the proposal of [13] and [20] and we reduced the SR parameter $\Delta$, hence weakening the strength of the SR scattering. In this case we could reasonably reproduce the experimental data at high $E_{\text{eff}}$ with both the Jacoboni ($\Delta = 0.34$ nm) and Takagi ($\Delta = 0.4$ nm) phonon parameters (open triangles) (Table 11). As stated above, the apparent disagreement at low $E_{\text{eff}}$ for both the strained and unstrained Si can be explained by a reduced experimental mobility in the first batch of devices. This interpretation is confirmed by the data extracted from the second batch of wafers. Indeed, Fig. 11 compares the mobility values of the sSi devices belonging to the first and second lot of wafers. The second batch do not present the roll-off in the mobility curve at low $N_{\text{inv}}$ and its mobility values well agree with simulations. For the simulations, we assumed the phonon parameters of [2] and $\Delta = 0.46$ nm and $\Delta = 0.4$ nm for the devices with Ge content of 20% and 27%, respectively.

In order to verify the assumption of reduced SR in strained silicon devices, in Fig. 12 we have simulated the mobility of the strained and unstrained Si samples at different operation temperatures. Using these curves to calculate $\mu_{\text{eff}}$, we have compared the experimental curve of the strained silicon devices, in Fig. 12 we have simulated the enhancement factor vs. temperature with the one obtained from simulations performed with the same SR parameters.

Fig. 10. Experimental and simulated $\mu_{\text{eff}}$ for the strained (open symbols) and unstrained silicon (filled symbols). To reproduce the experimental data of sSi, the simulations must assume a reduced SR.

Fig. 11. Comparison between the mobility values of devices belonging to the first and second lot of wafers. The second batch do not present the roll-off in the mobility curve at low $N_{\text{inv}}$ and its mobility values well agree with simulations. For the simulations, we assumed the phonon parameters of [2] and $\Delta = 0.46$ nm and $\Delta = 0.4$ nm for the devices with Ge content of 20% and 27%, respectively.

Fig. 12. Simulated mobility for the unstrained (left) and strained (right) Si devices for different operation temperatures.
used to fit the data of strained and unstrained silicon devices in Fig. 10.

Fig. 13 shows the results at large \( E_{\text{eff}} = 1.2 \text{ MV/cm} \) for various temperatures. Here we see that the strong EF reduction with decreasing \( T \) is not reproduced by the numerical model. In fact the simulated EF is rather constant, while the measured one shows a strong decrease for \( T < 200 \text{ K} \). [22].

5. Discussion and conclusions

By characterizing the electron mobility enhancement obtained in silicon with different strain levels, we found that the measured mobility enhancement at 300 K is independent of the inversion charge concentration, thus it is the same for medium and large \( E_{\text{eff}} \). Moreover the mobility enhancement factor due to strain presents a linear dependence on the Ge content of the device substrates, hence on the level of strain in the channel, and no saturation effect can be seen in our data.

Characterization of the strained and unstrained samples versus temperature showed a decrease of the enhancement factor independent of temperature above 200 K, but, for \( T < 200 \text{ K} \), EF decreases at both low and high \( E_{\text{eff}} \). While a decrease in the EF value at medium \( E_{\text{eff}} \) has been predicted by models based on phonon scattering [2], the reduction at large \( E_{\text{eff}} \) seems difficult to interpret.

Mobility simulations performed with state of the art models could reproduce the experimental data at room temperature only by assuming a reduced SR scattering for the strained devices. However, the experimental temperature dependence of the EF is not correctly reproduced by the simulations, and these findings suggest that the assumption of a reduced SR in strain silicon devices is not fully justified. In fact the change of SR intensity leads to an enhancement factor that shows a weak dependence on the operating temperature, while the mechanism responsible for the strong reduction in the EF for low \( T \) should exhibits a larger temperature dependence to reproduce the experimental SR limited mobility.

Our findings show that the description of the mobility in strained Si at large \( E_{\text{eff}} \) provided by the state of the art SR models is not adequate. Furthermore, it is worth noting that more sophisticated models for the channel quantization that could take into account for effects like the wave-function penetration may show a reduced energy splitting between the 2-fold and 4-fold subbands in the unstrained silicon channels. In such a condition, the beneficial effect of strain induced valley splitting could also be experienced in strong inversion, where mobility is limited by SR.

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