Investigation of Hot Carrier Stress and Constant Voltage Stress in High-κ Si-Based TFETs

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Abstract—This paper reports the experimental investigation of hot carrier stress (HCS) and constant voltage stress (CVS) in high-κ Si-based tunnel FETs. For the devices in this paper, due to the large injection of cold carriers and to the presence of traps in the gate dielectric, the degradation of the transfer characteristics under CVS is much more severe than under HCS. The experimental results show that the sub-threshold swing remains stable under both HCS and CVS conditions, and it is not influenced by the stress-induced increase of the interface trap density.

Index Terms—Tunnel FET, hot carrier stress, constant voltage stress, high-κ dielectric.

I. INTRODUCTION

Tunnel field effect transistors (TFET) have attracted much attention due to their possibility to offer a sub-60 mV/dec sub-threshold swing (SS) [1], [2]. Many investigations have been carried out to improve the characteristics of TFET by modifying the device structure, introducing new materials, or improving the fabrication technology [3]–[7]. Limited attention has been paid so far to the reliability of TFETs.

Initial studies on TFET reliability were based on n-type transistors with SiO2 gate dielectric [8], where the degradation of I–V characteristics was more severe under hot-carrier stress (HCS) than under constant voltage stress (CVS). In TFETs, HCS is due to the injection of hot carriers at the source/channel junction resulting from the strong electric field, while in conventional MOSFETs, the hot carrier injection occurs near the drain end [9]. Referring to the existing studies on MOSFETs, after replacing the gate stacks with high-κ dielectrics, the hot-carrier reliability of nMOS transistors worsens, because the oxide barrier is much lower and the trap density is higher [10].

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II. DEVICE AND EXPERIMENT DESCRIPTION

Si-based TFETs were fabricated by CEA/LETI, France, using a 100 nm fully depleted SOI-CMOS compatible process flow [see Fig. 1(a)]. The gate dielectric is a 3 nm HfO2 layer. Additional details of the device processing can be found in [4]. We have applied stress with time ranging from 10 to 10000 s, performing either HCS (Vg = Vd = 2.5 V, Vs = 0 V) or CVS (Vg = 2.5 V, Vd = Vs = 0 V) [see the energy bands in Fig. 1(b)]. Alternated to stress, both DC and pulsed I–V measurements have been performed at room temperature to study the influence of stress on the I–V characteristics.

In fact, although the working principle of TFETs is based on BTBT, TAT will inevitably contribute to the total drain-source current. As illustrated in Fig. 1(c), TAT is activated by the traps with energy levels located in the forbidden Si bandgap, and consists of the electrons coming from the valence band in the...
source that get trapped in the forbidden bandgap and then are re-emitted to the conduction band of the channel [17]. With $V_d = 1$ V and source grounded, the gate was pulsed at 10 kHz and 500 kHz with a 100 ns edge time and a 50% pulse duty cycle. The base voltage of the gate pulse was 0 V, whereas the amplitude voltage was swept from 0 to 2.5 V. For each data point, the measurements were repeated 5 times to obtain an average value. In this way, since the whole process is expected to take more than $1 \mu$s [18], TAT is expected to be substantially suppressed at high pulse frequency and BTBT can be better detected since it is no longer masked by TAT [15], [16].

The TFETs are floating-body SOI devices in this study, so the feasibility of performing charge pumping measurements should be evaluated first [19]. When pulsing the gate with a squared waveform of constant base level and amplitude, the drain and source were maintained at the same potential that was swept across a suitably chosen range from 0 to 1.5 V, in order to activate the generation-recombination process at the Si/gate dielectrics interface. The current measured at the $P^+$ source contact was found to be proportional to the frequency of the gate pulses, proving the correctness of the charge pumping setup [20], [21]. Thus, even in the absence of the body contact in our SOI-based TFETs, since the source and drain feature opposite doping type, we could still perform charge pumping measurements to evaluate $N_{it}$. For the charge pumping results presented below, the gate was driven with a 500 kHz square waveform with the edge time of 100 ns, the amplitude of 1.5 V, the base level of 0 V and a pulse duty cycle of 50%.

In this paper, TFETs with different geometries have been characterized and consistent trends and similar absolute values of the degradation have been observed. Thus, in the following discussions, only the results of a few typical TFETs are presented.

### III. Results and Discussion

#### A. Hot Carrier Stress

The transfer characteristics of a 10/0.1 $\mu$m TFET before and after different time steps of HCS are shown in Fig. 2. In this paper, two $V_{gs}$ at different drain currents are chosen as the indicators to monitor the characteristics shift during stress, namely $V_{th,1}$ ($V_{gs}$ at $I_{ds} = 2$ pA/µm) and $V_{th,2}$ ($V_{gs}$ at $I_{ds} = 0.2$ nA/µm) [4]. Fig. 2(a) shows the results from DC measurements, where only a small shift of the characteristics (within 40 mV) can be observed. Fig. 2(b) shows the results of the 500 kHz pulsed $I$–$V$ tests. The comparison between the transfer characteristics of the fresh TFET with DC and 10 kHz pulsed $I$–$V$ tests. The comparison between the transfer characteristics of the fresh TFET with DC and 10 kHz pulsed $I$–$V$ tests are presented, too. It can be seen that TAT is substantially suppressed at 500 kHz: the sub-threshold characteristics are much steeper than in DC. Indeed, the actual BTBT current is no longer masked by the TAT-induced leakage current. The values of $\Delta V_{th,1}$ and $\Delta V_{th,2}$ obtained from the DC and the pulsed $I$–$V$ tests are extracted and shown in Fig. 3. The shifts of the pulsed $I$–$V$ curves are similar to the DC case.
Fig. 3. Experimental values of $\Delta V_{th,1}$ and $\Delta V_{th,2}$ after HCS extracted from DC, 10 kHz, and 500 kHz pulsed $I-V$ characteristics (see Fig. 2).

Fig. 4. Subthreshold swing of the TFET before and after HCS, as a function of $I_{ds}$: (a) DC; (b) 500 kHz pulsed $I-V$ measurements.

Fig. 5. Charge pumping current as a function of the drain and source voltages ($V_d = V_s$) before and after HCS up to 10000 s.

Fig. 6. Transfer characteristics of the TFET before and after 10000 s HCS stress using forward and reverse sweeps: negligible hysteresis can be observed.

The corresponding SS as a function of the drain current is shown in Fig. 4. The SS values extracted from DC are much larger than the 60 mV/dec for both fresh and stressed TFET [see Fig. 4(a)]. After HCS, a slight improvement in SS was observed in the very low drain current region ($I_{ds} < 10^{-13}$ A/µm). On the other hand, SS in 500 kHz pulsed curves is smaller than 60 mV/dec at low drain current [see Fig. 4(b)], consistently with the findings in [16] where the SS from pulsed measurements is lower than from DC measurements. From the characteristics in Fig. 2(b), we can observe a small improvement in SS in the 500 kHz $I-V$ test, this small improvement is not visible in the SS $- I_{ds}$ plot in Fig. 4(b).

Therefore, based on the discussions above, the small improvement of SS in the DC curves appears to be due to the impact of HCS on TAT, not on BTBT. Generally speaking, in this study, the TFET SS is robust to HCS and this may be due to the limited hot electrons density under HCS ($I_{ds}$ is about 1 nA/µm).

During the HCS, the peak value of charge pumping current $I_{cp,max}$ increased progressively, suggesting an increase in $N_{it}$ (see Fig. 5), which is estimated as

$$N_{it} = I_{cp,max} / (f \cdot q \cdot A_g) \quad (1)$$

where $f$ is the pulse frequency, $q$ is the unit charge, and $A_g$ is the gate area [23].

After 10000 s HCS, $N_{it}$ increases from $6.8 \times 10^{10}$ cm$^{-2}$ to $7.2 \times 10^{10}$ cm$^{-2}$. It’s worth noting that this is the average value for $N_{it}$ and not the peak density for the localized interface traps. Correspondingly, Fig. 6 shows the transfer characteristics for both forward and reverse quasi-static sweeps. For the $V_g$ swept from 0 V to 2.5 V, the electron filling factor of interface traps is inclined to be lower than for $V_g$ swept from 2.5 V to 0 V [8], which makes hysteresis an indicator for interface traps. The negligible hysteresis after 10000 s HCS suggests that the influence of the interface trap, even after they increase due to stress, is very limited.
B. Constant Voltage Stress

The transfer characteristics of a TFET before and after CVS are reported in Fig. 7. The shifts of the curves are quite visible. From Fig. 8, the increases in $V_{th,1}$ and $V_{th,2}$ extracted from DC, 10 kHz, and 500 kHz pulsed I–V are similar, suggesting that the degradation in the transfer characteristics is mainly due to the oxide trapped charge and/or increase in $N_{it}$. The increase in both $V_{th,1}$ and $V_{th,2}$ are more evident than under HCS.

Concerning $N_{it}$, the charge pumping currents before and after CVS are presented in Fig. 9. Under CVS, there is a significant voltage shift between the $I_{cp}$ curves related to the fresh and stressed device. By considering the increases of $V_{th,1}$ and $V_{th,2}$ due to CVS, and by shifting the $I_{cp}$ curves after stress by the same $\Delta V_{th}$, the stressed curve shows an increase in magnitude comparing to the fresh one. $N_{it}$ increases by $6 \times 10^9$ cm$^{-2}$ (from $4.0 \times 10^{10}$ cm$^{-2}$ to $4.6 \times 10^{10}$ cm$^{-2}$), a value comparable with that found after HCS. Fig. 10 presents the transfer characteristics before and after 10 000 s CVS using forward and reverse sweeps, where negligible hysteresis can be observed, suggesting again the limited contribution of interface traps.

Therefore, $\Delta V_{th}$ should be attributed to the negative trapped charge in the gate oxide, deriving from the trapping of hot and/or cold electrons. The electric field near the source/channel junction is stronger under HCS than under CVS [see Fig. 1(b)]. Hence, hot electrons trapping more likely occurs under HCS.

Fig. 11 presents SS as a function of the drain current. After including the influence of statistical errors, we do not see any clear dependence of SS on the stress time, for both DC and pulsed I–V measurements.

C. Discussion

From the results above, the degradation in the transfer characteristics is more severe under CVS than under HCS. Referring to [24], under HCS, the hot electrons are accelerated by the longitudinal field component parallel to the channel direction and injected close to the source/channel junction. However, under CVS, the degradation is mainly due to the cold electron
injection determined by the vertical field component perpendicular to the channel surface. The $V_{th}$ increase in both DC and pulsed $I–V$ measurements indicates the buildup of negative charge in the oxide, and the trapping of cold electrons plays an important part in the stress effects of the high-κ Si-based TFET.

To understand the relationship between the stress-induced degradation and cold electrons injection, several different bias conditions during stress were chosen for comparison. Fig. 12 presents $\Delta V_{th}$ after 1000 s stress as a function of the normalized gate current density during stress ($J_{g,\text{stress}}/J_{g,\text{ref}}$), where $J_{g,\text{ref}}$ corresponds to 2.5 V HCS. The gate current is fairly constant during the stress experiments (see Fig. 12). It can be seen clearly that more gate leakage during stress induces a stronger degradation, proving that the main factor of inducing the shifts in characteristics should be the trapping of cold electrons. No direct evidence of hot carriers injection can be observed in the results of degradation under 2.5 V HCS. Although the degradation under 3 V HCS is stronger than that under 2.5 V HCS, it is hard to attribute that to the hot carrier injection, since the cold electrons injection becomes larger.

Since it was not possible to further increase the voltage during HCS without possible breakdown, nMOS transistors fabricated with the same process were analyzed in this study, to help evaluating the damage due to hot carriers injection.

Fig. 13 reports $\Delta V_{th}$ as a function of the stress time for both TFETs and MOSFETs. Under 3 V CVS, a smaller $\Delta V_{th}$ could be observed for the nMOSFET due to a weaker cold electrons injection, which is proved by the fact that $J_{g,\text{stress}}$ of the nMOSFET was half that of the TFET under 3 V CVS. For nMOSFETs, $\Delta V_{th}$ under 3 V HCS is larger than that under 3 V CVS, suggesting a big contribution of hot carriers injection. Furthermore, under 3 V HCS, $\Delta V_{th}$ of the nMOSFET is much larger than the value of the TFET (370 mV and
40 mV, respectively, after a stress of 1000 s). This difference suggests a much stronger hot carrier injection for the nMOSFET, which can be due to difference in the electric field or the density of hot carriers. For TFET, the electric fields close to the source/channel junction and parallel to the channel direction are higher than at the drain end of nMOSFET under similar condition. So the hot carrier density should be the main reason responsible for the degradation differences.

In this paper, the ON-state current of TFET is very small (about 1 nA/μm). TFETs with larger ON-state current per unit width, hence larger hot carrier fluxes, may actually exhibit more prominent hot carrier degradation.

Since SS is a very important performance indicator of TFET, the evolution of SS under stress tests should be further investigated. In this paper, the increases in interface trap density are not very large under both HCS and CVS. To investigate the influence of larger ΔN_{it} on SS, the degradation of a 10/0.2 μm p-type TFET under negative CVS (V_g = −2.5 V, V_D = V_T = 0 V) was investigated. The value of N_{it} increased from 1.0 × 10^{11} cm⁻² to 1.3 × 10^{11} cm⁻² (ΔN_{it} = 3 × 10^{10} cm⁻², whereas ΔN_{it} = 4 × 10^9 cm⁻² for the n-type TFET under HCS condition). Although the increase in N_{it} was larger, there was no visible degradation in the transfer characteristics (see Fig. 14) and no change in the SS−I_{ds} characteristics (see Fig. 15). However, in our previous study, radiation effects of TFETs exposed to 10-keV X-ray have been investigated, and an SS increase could be observed at ΔN_{it} = 2 × 10^{11} cm⁻² [25]. These findings suggest that N_{it} increase may change TFET SS region, but the electrical stress-induced limited N_{it} increase is too small to induce visible changes.

IV. CONCLUSION

The effects of HCS and CVS on high-κ Si-based TFETs have been investigated. The bias stress effects in TFETs with high-κ gate dielectrics are different from conventional MOSFETs and TFETs with SiO₂ gate dielectrics.

In this paper, the degradation of the TFET transfer characteristics under CVS is much more severe than under HCS, due to the strong injection of cold carriers overwhelming the hot carriers injection. This conclusion is different from that in [4], where more severe degradation was observed under HCS for TFETs with SiO₂ gate dielectrics, suggesting more traps existing in high-κ dielectrics. Meanwhile, this is also due to the small ON-state current of the TFET in this study. If the ON-state current would be significantly increased, a strong degradation of TFET might be observed under HCS.

No increase in SS has been observed under both HCS and CVS, meaning that the SS behavior is not appreciably influenced by the limited stress-induced increase in N_{it}.

REFERENCES


Authors’ photographs and biographies not available at the time of publication.